

Compal Confidential

EL4C1 & EL451 (C340/S540-14)

DIS M/B Schematic Document

Intel Whiskey Lake Processor with DDR4

MX110 (23x23mm)

2018-10-18

LA-H081P

REV : 0 . 3

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title Cover Page		
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Voltage Rails

power plane	B+	+5VALW +3VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +1.05VS_VCCSTG +VCC_CORE +VCC_GT +VCC_SA +1.05VS_VCCIO +1.8VS +0.6VS
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
DIS Only Components	DIS@
UMA Only Components	UMA@
HDMI Logo	45@
Touch Screen	TS@
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
GPU GC6 Components	GC6@
Un-Mount GPU GC6 Components	NOGC6@
Colay SATA/PCIE on M2	SSD_DET@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
Test Point	TP@
Keyboard BackLight	KBL@ NOKBL@
Project select	S540@ S340@ C340@
OneKeyBattery	ONEKEY@ NON_ONEKEY@
Intel CNVi	CNVi@ NONCNVi@
GPU select	N17S_G0@ N17S_G2@ N16S@ N17S@
Connectors	ME@

Item	BOM Structure
X4E	X4ES540@ X4EC340@
On Board RAM	MD@
no On Board RAM	NO_MD@
On Board RAM X76 Resistors	X76RAM@
DRAM (Hynix 4GB)	H4G_S540@
DRAM (Micron 4GB)	M4G_S540@ S4G_S540@
VRAM (Hynix 4GB)	H4G_VRAM@ H4G@ H4G_R1@ H4G_R3@
VRAM (Samsung 4GB)	S4G_VRAM@ S4G@ S4G_R1@ S4G_R3@
VRAM (Micron 4GB)	M4G_VRAM@ M4G@ M4G_R1@ M4G_R3@

USB 2.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

USB 3.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	
5	
6	

PCIe Port Table

Port	Lane	
1		
2		
3		
4	0	
5	0	
6	1	
7	2	
8	3	
9	3	
10	2	
11	1	
12	0	
13	0	
14	0	
15	1	
16	0	

SATA Port Table

Port	External SATA Port
0	
1A	SSD1
1B	
2	SSD2

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011x 16h	NCT778W	1001 100x 98h
		thermal sensor	1001 101ab 21h

PCH SM Bus address GPU SM Bus address

Device	Address	Device	Address
DDR_0JIMM1	1010 000x A0h	Internal thermal sensor	1001 111x 9Eh
Touch_Pad			

SMBUS Control Table

	SOURCE	DGPU	BATT	CHARGER	NECP388	SODIMM	TP	PCH	G-SENSOR	THM sensor
EC_SMB_CK1 EC_SMB_DA1	NECP388 +3VL	X	+3VALW	+19V_VIN	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	NECP388 +3VS	X	+3VS	X	+3VS	X	X	+3VS	X	+3VS
EC_SMB_CK4 EC_SMB_DA4	NECP388 +3VS	X	X	X	X	X	X	X	+3VS	X
SOC_SMBCLK SOC_SMBDATA	PCH +3VALW	X	X	X	X	+3VS	+3VS	X	X	X
SOC_SML0CLK SOC_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	PCH +3VS	X	X	X	+3VS	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF

CPU

UC1 I3 8145U@ QOK9 W0 2.1G BGA SA0000C0R20	UC1 I5 8265U@ QQTG W0 1.6G BGA SA0000C0R20	UC1 I7 8565U@ QOK6 W0 1.8G BGA SA0000C0R20
UC1 I3 8145U_R3@ SRD1V W0 2.1G SA0000C0R30	UC1 I5 8265U_R3@ SREJ3 W0 1.6G SA0000C0R30	UC1 I7 8565U_R3@ SREJP W0 1.8G SA0000C0R30

PCB

ZZZ PCB@ PCB 2GA LA-H081P REV0 MB 4 DA8051HA000

X4E X4E_S540_14

ZZZ X4ES540@ X4E_S540_14 X4EAT63BL5T
--

X4E_C340_14

ZZZ X4EC340@ X4E_C340_14 X4EAT63BL0T
--

GPU

UV1 N17S_G0@ N17S-G0-A1 SA0000CC000	UV1 N17S_G2@ N17S-G2-A1 SA0000CC000
---	---

DRAM S540

ZZZ S4G_S540@ K4A8G18WC-BCTD X768053BL05	ZZZ H4G_S540@ HSAN8G9NCR-KVC X768053BL04	ZZZ M4G_S540@ MT40A51TAM18LY-075:E X768053BL05
--	--	--

VRAM S540

ZZZ VH4G_S540@ H5GC8H24AJR-R2C X768053BL01	ZZZ VM4G_S540@ MTS1J256M32HF-80:B X768053BL03
--	---

DRAM C340

ZZZ3 S4G_C340@ K4A8G18WC-BCTD X768053BL05	ZZZ3 H4G_C340@ HSAN8G9NCR-KVC X768053BL04	ZZZ1 M4G_C340@ MT40A512M18LY-075:E X768053BL05
---	---	--

VRAM C340

ZZZ VH4G_C340@ H5GC8H24AJR-R2C X768053BL01	ZZZ VM4G_C340@ MTS1J256M32HF-80:B X768053BL03
--	---

-PowerMap_KBL_DDR4_Volume_NON CS]



G3->S0

S0->S3/DS3

S0/DS3->S0

S0->S5

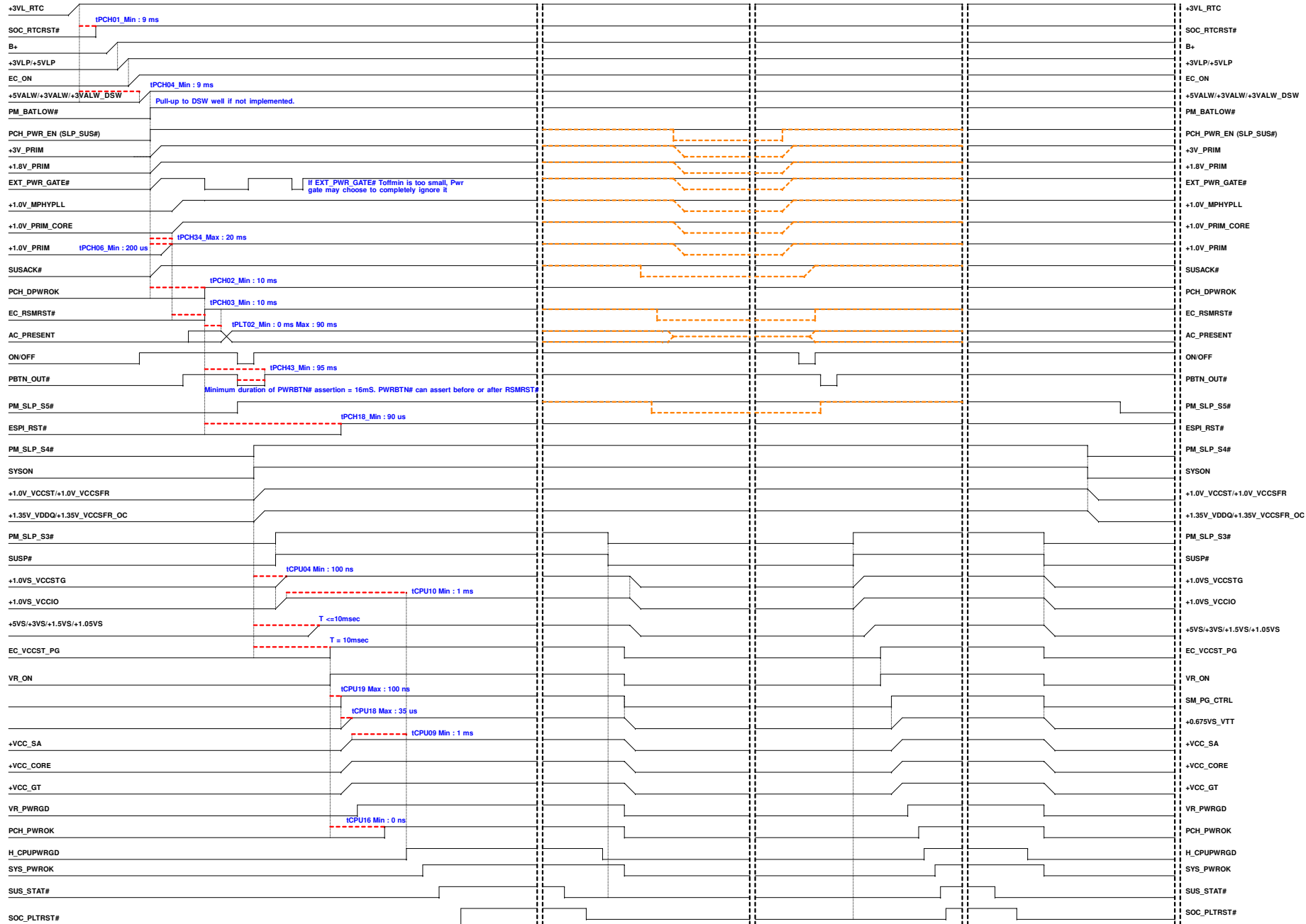
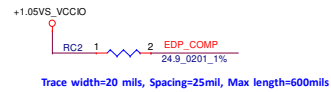


Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

< Compensation PU For eDP >

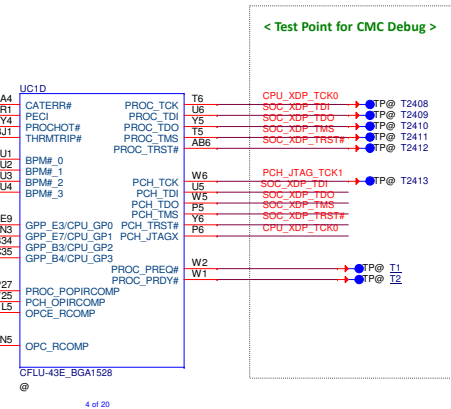
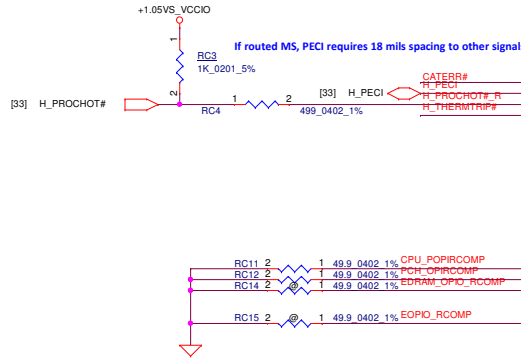
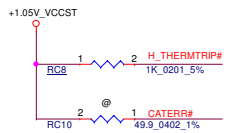
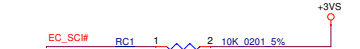
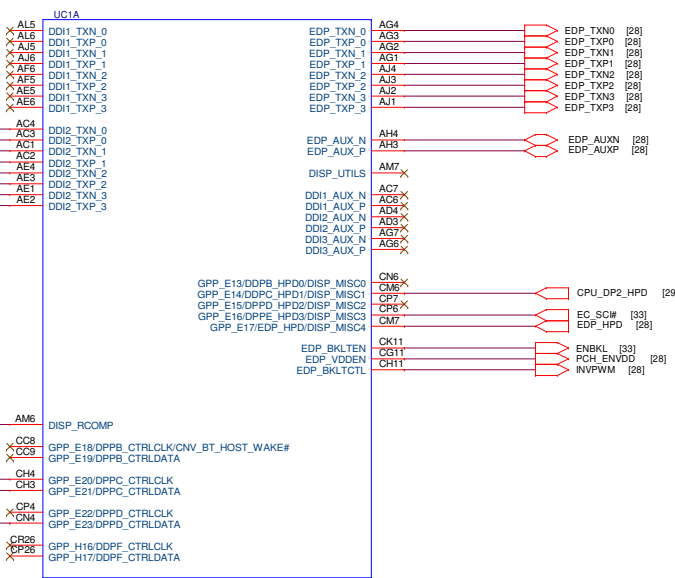


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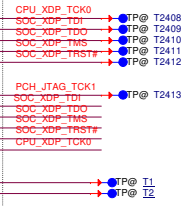
HDMI DDC (Port 2)

- [29] CPU_DP2_CTRL_CLK
- [29] CPU_DP2_CTRL_DATA
- [28] TS_I2C_RST#

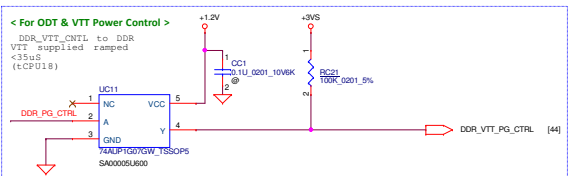
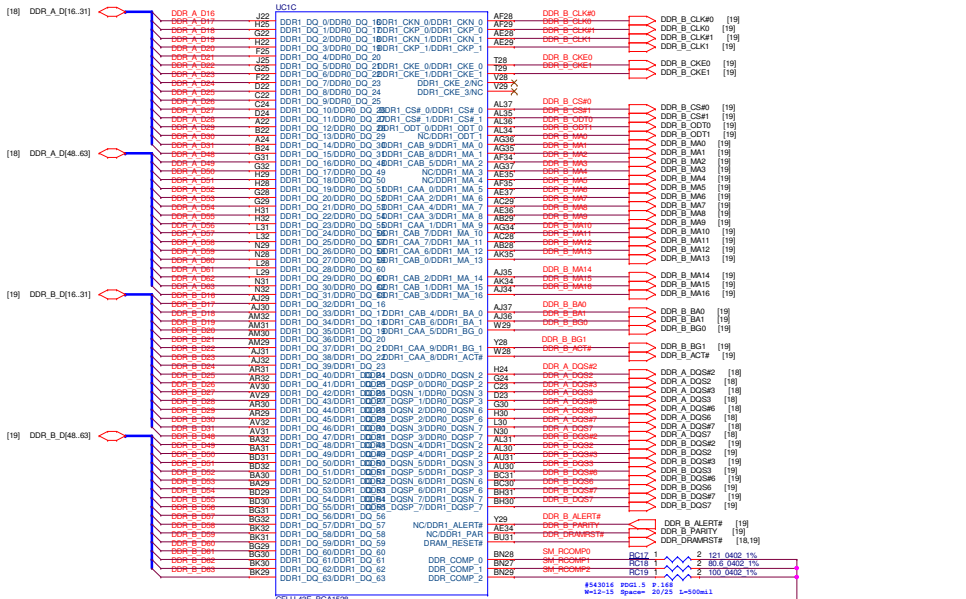
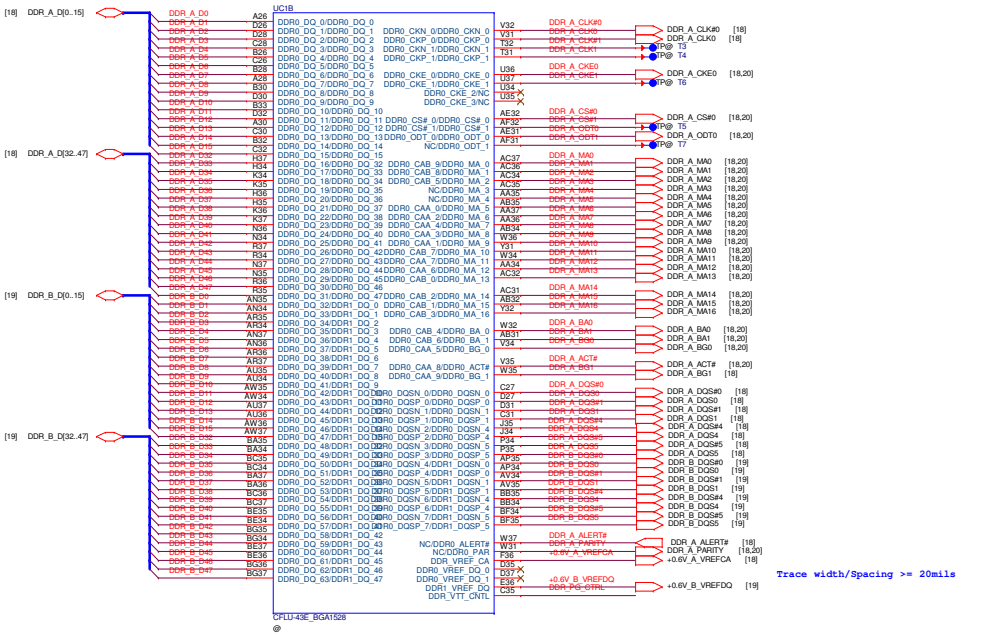
EDP_COMP



< Test Point for CMC Debug >

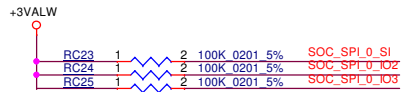


Non-Interleaved Memory



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Date				Monday, October 29, 2018

Note: The internal pull-up is disabled when RSMRST# is asserted (during reset) and only enabled after RSMRST# de-assertion



SML1ALERT#/
PCHHOT#/GPP_B23

- If USB 3.1 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.
- If USB 3.1 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float.
- If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.

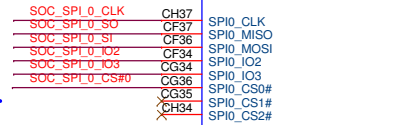
SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

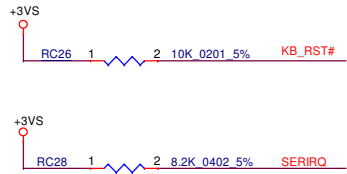
SPI ROM



5 of 20

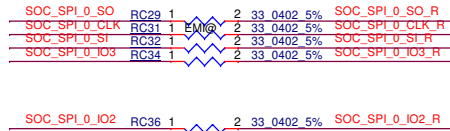
SMB
(Link to DDR)

SML1
(Link to EC, DGPU, Thermal Sensor)

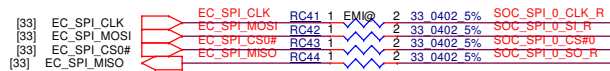


RPC1, RPC3 and RC30 are close to UC3

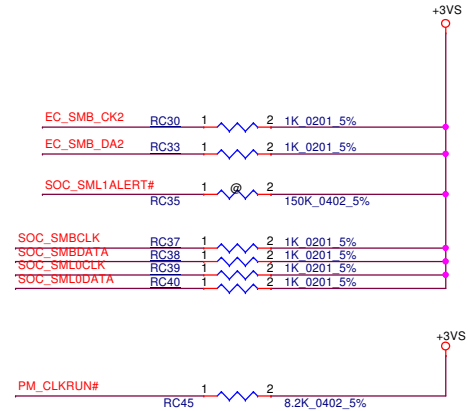
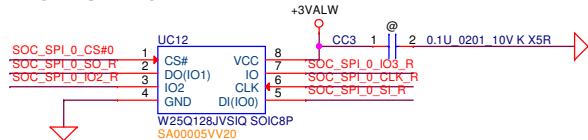
From SOC



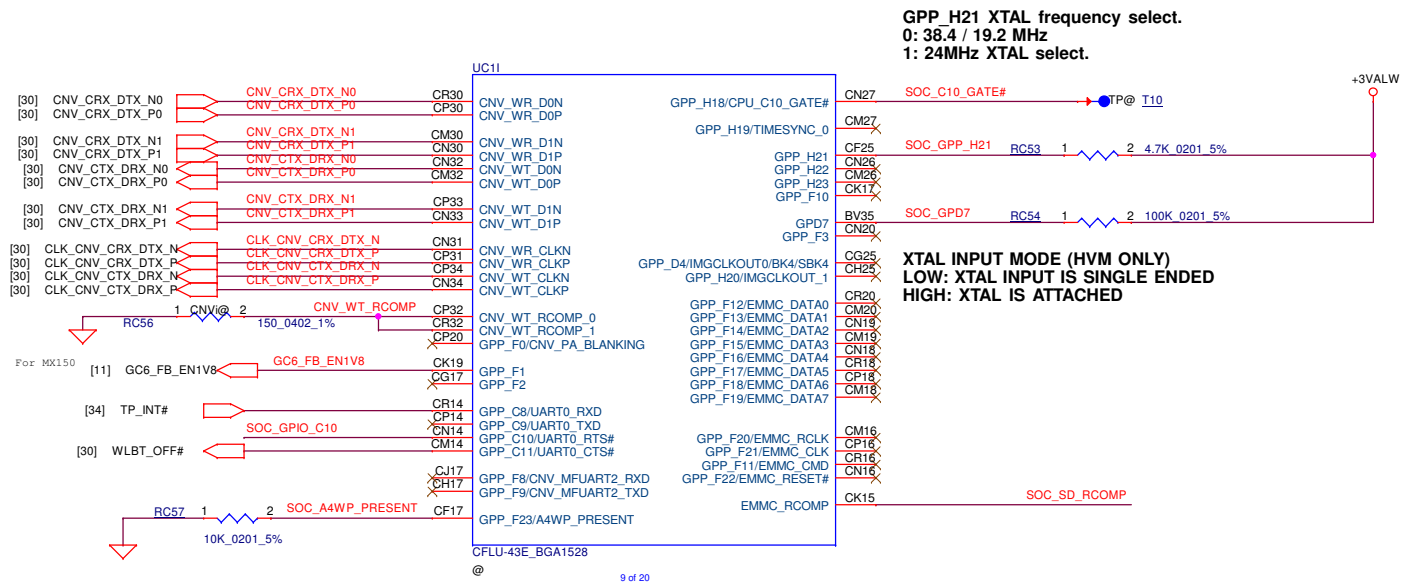
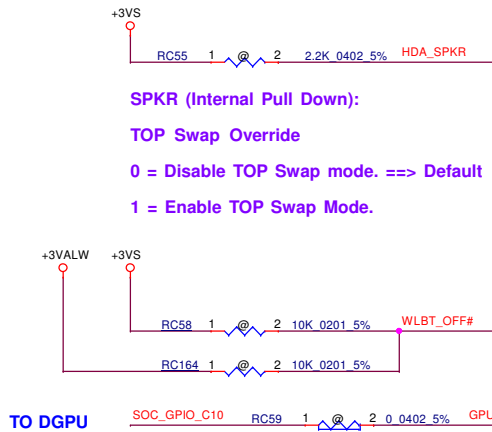
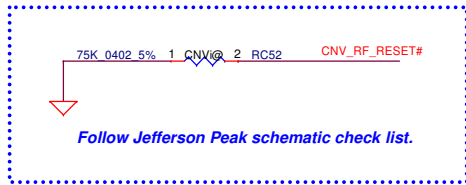
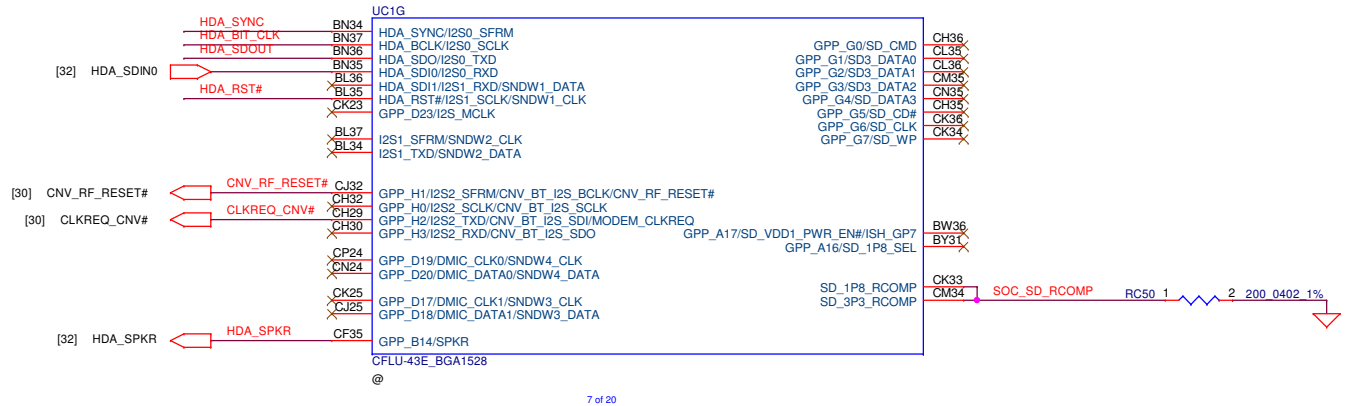
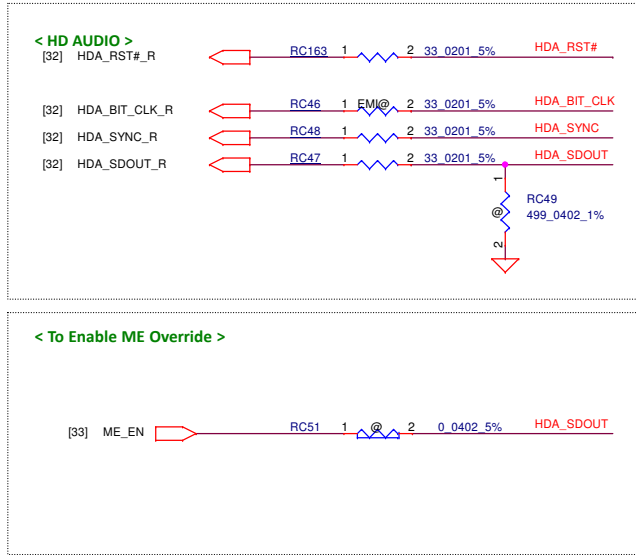
From EC



< SPI ROM - 16M >



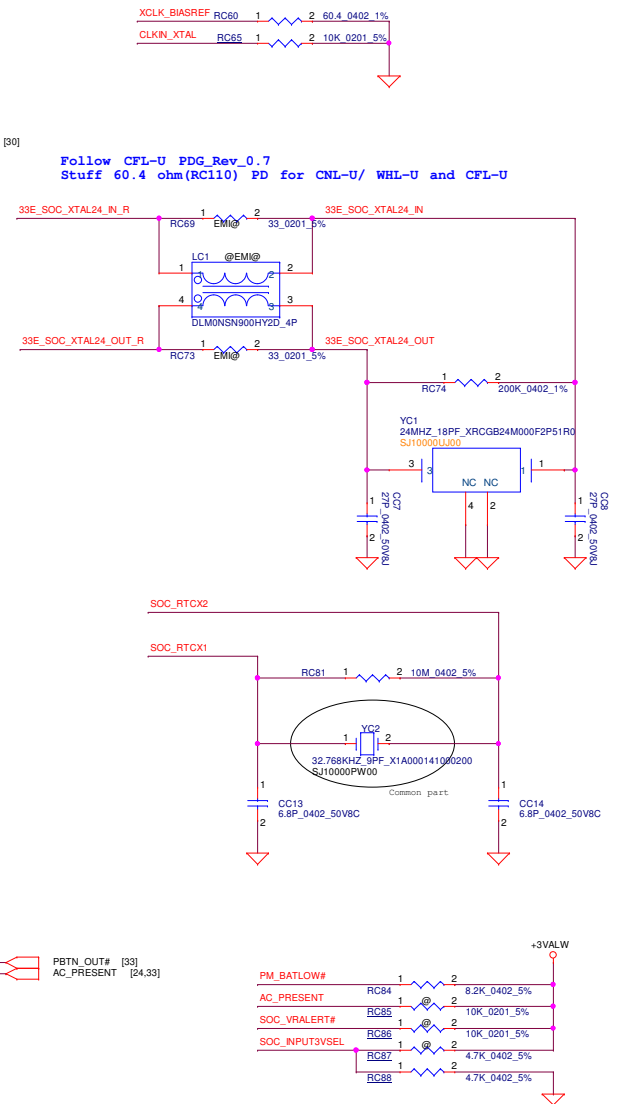
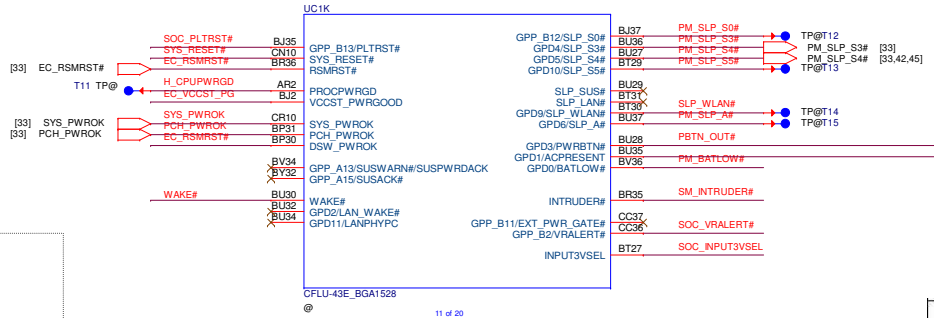
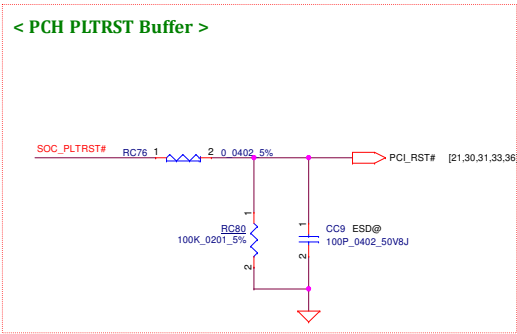
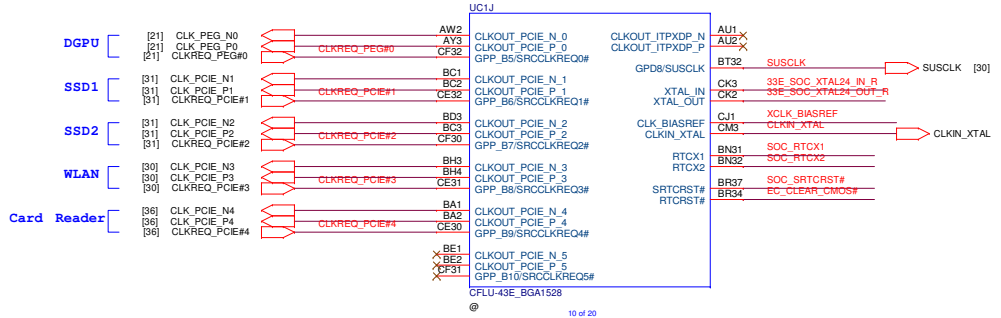
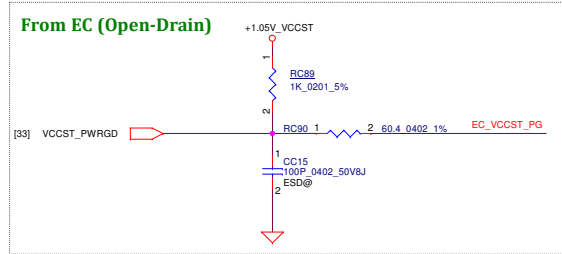
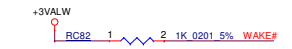
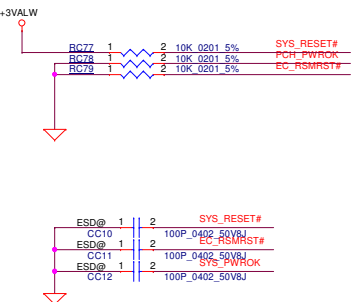
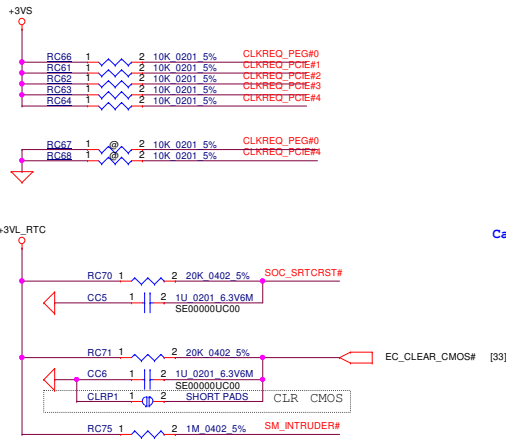
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Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	WHL-U(3/12)SPI,SMB,LPC,ESPI
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GPP_H21 XTAL frequency select.
0: 38.4 / 19.2 MHz
1: 24MHz XTAL select.

XTAL INPUT MODE (HYM ONLY)
LOW: XTAL INPUT IS SINGLE ENDED
HIGH: XTAL IS ATTACHED

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INPUT3VSEL	I	Strapped high if PCH's VCCDSW_3P3 rail is 3.0V +/- 5%; else PCH's VCCDSW_3P3 rail is 3.3V +/- 5%. This pin is in the VCCPRIM_3P3 well. Note: When strapped for 3.0V operation, it is expected that the rest of the platform's 3.3V rails are at 3.0V (e.g. the battery is a 1S configured battery) and that components can function properly at 3.0V.
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GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

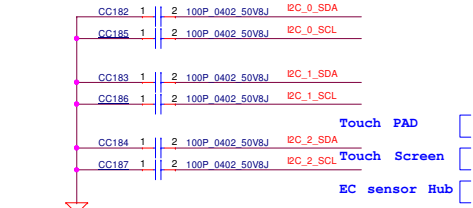
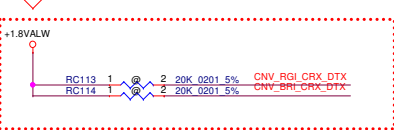
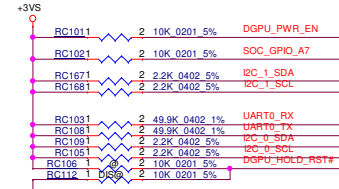
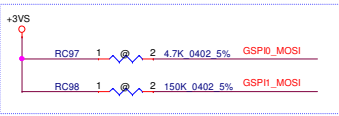
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This functi on is us ed if when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode

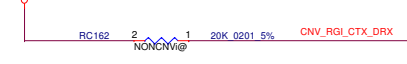


PCH EDS : M.2 CNV Mode Select

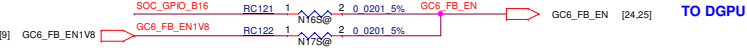
GPP_F6/CNV_RGI_DT

0 = Integrated CNVi enable.

1 = Integrated CNVi disable.

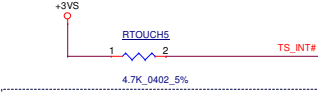
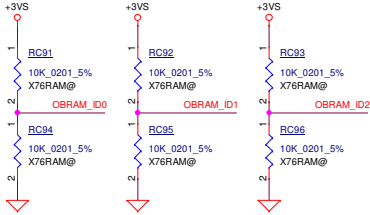


CNVi RGI_DT pin gets the pull-down resistor (1K ohm) from the internal CRF module when CNVi is enabled. There must not be any pull-down resistor connected on the board.

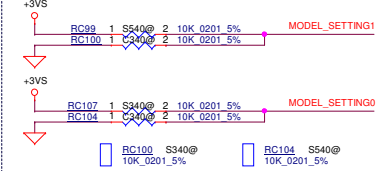


Capacity	Description	X76	PART NUMBER (R1)	GPP_B19 OBRAM_ID0	GPP_B20 OBRAM_ID1	GPP_B21 OBRAM_ID2
4GB	WITHOUT ON-BOARD RAM	N/A	N/A	0	0	0
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) EL451	X7680638L05	SA0000B6F00	0	0	1
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) EL4C1	X7680538L06	SA0000B6F00	0	0	1
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) EL451	X7680638L04	SA0000BMN00	0	1	0
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) EL4C1	X7680538L04	SA0000BMN00	0	1	0
	MICRON 2666MHz (MT40A512M16LY-075:E) EL451	X7680638L06	SA0000ARD20	0	1	1
	MICRON 2666MHz (MT40A512M16LY-075:E) EL4C1	X7680538L05	SA0000ARD20			
	N/A	N/A	N/A			

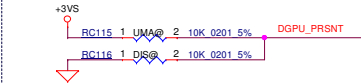
RC94 NO_MD@ 10K_0201_5% RC95 NO_MD@ 10K_0201_5% RC96 NO_MD@ 10K_0201_5%



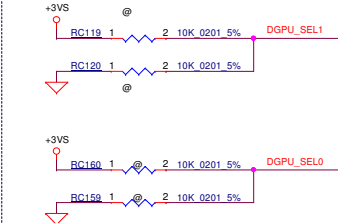
Function	MODEL_SETTING1 (GPP_D12)	MODEL_SETTING0 (GPP_D11)
C340	0	0
S340	0	1
S540	1	0



Function	DGPU_PRNST (GPP_C15)
DIS	0
UMA Only	1

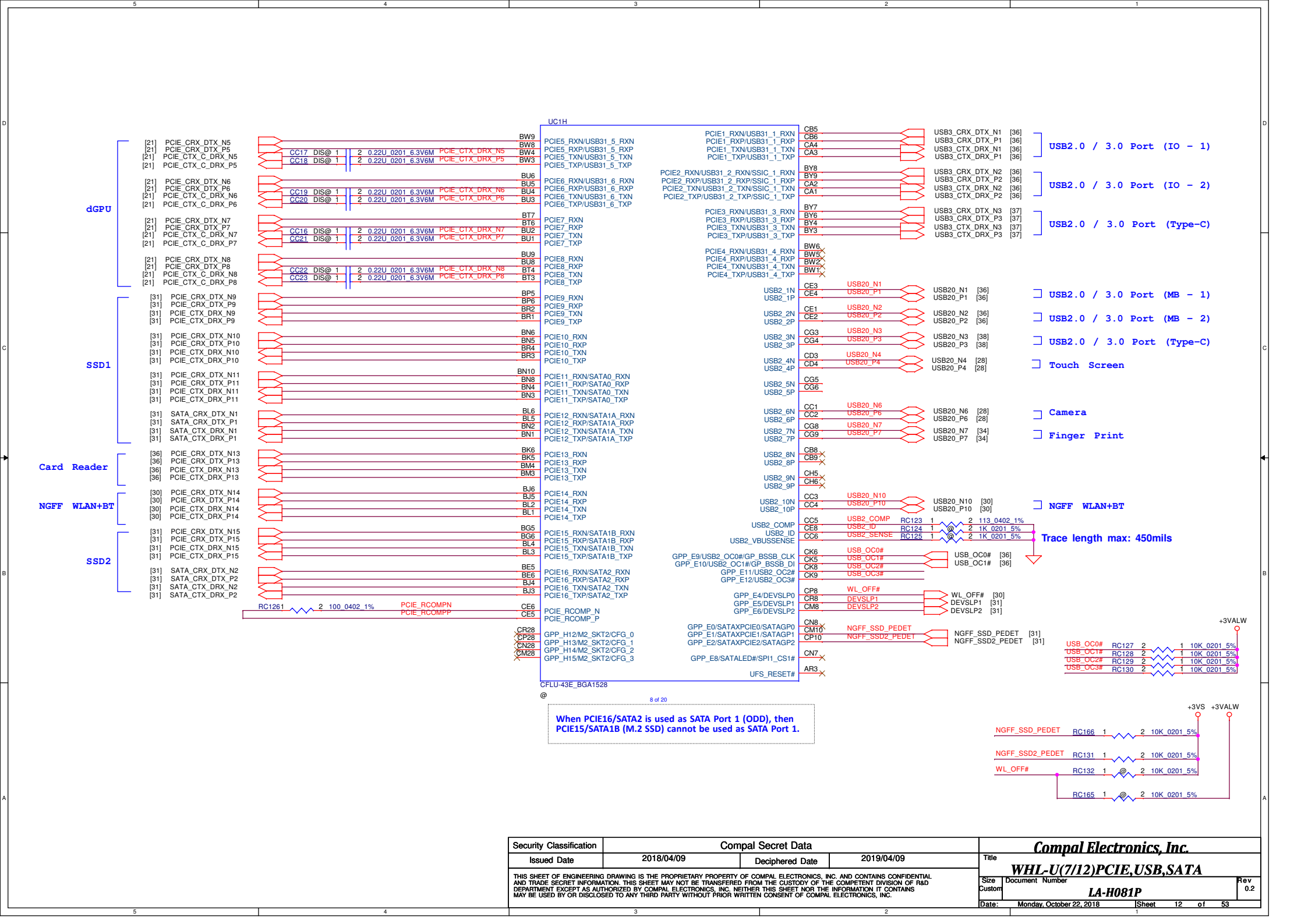


Function	MODEL_SETTING2 (GPP_A20)
Array MIC	1
Single MIC	0

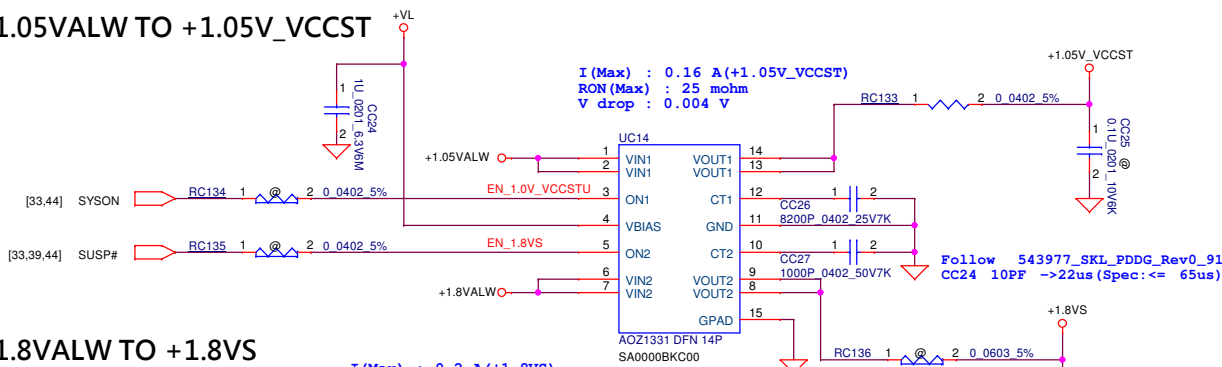


[9] G6_FB_EN1V8 G6_FB_EN1V8 RC121 1 N16S@ 2 0 0201 5% G6_FB_EN G6_FB_EN [24,25] TO DGPU

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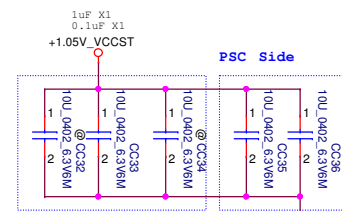
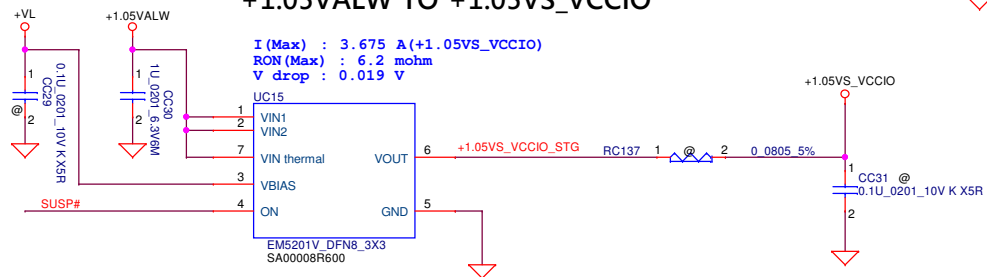
+1.05VALW TO +1.05V_VCCST



+1.8VALW TO +1.8VS

I(Max) : 0.2 A(+1.8VS)
RON(Max) : 25 mohm
V drop : 0.005 V

+1.05VALW TO +1.05VS_VCCIO



Close to BP11 & BP2

Close to BR11 & BT11

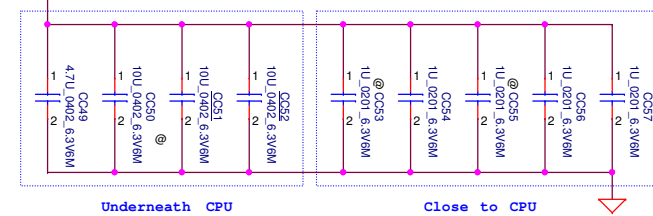
Close to BM26

Close to BG1 & BG2

change package of 1U from 0201 to 0402

PSC Side

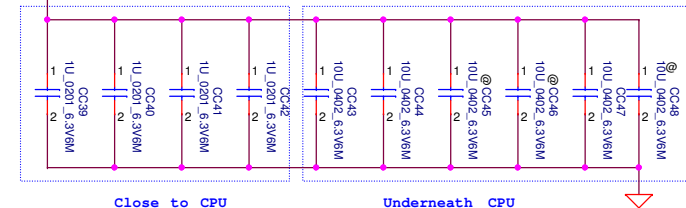
BSC Side



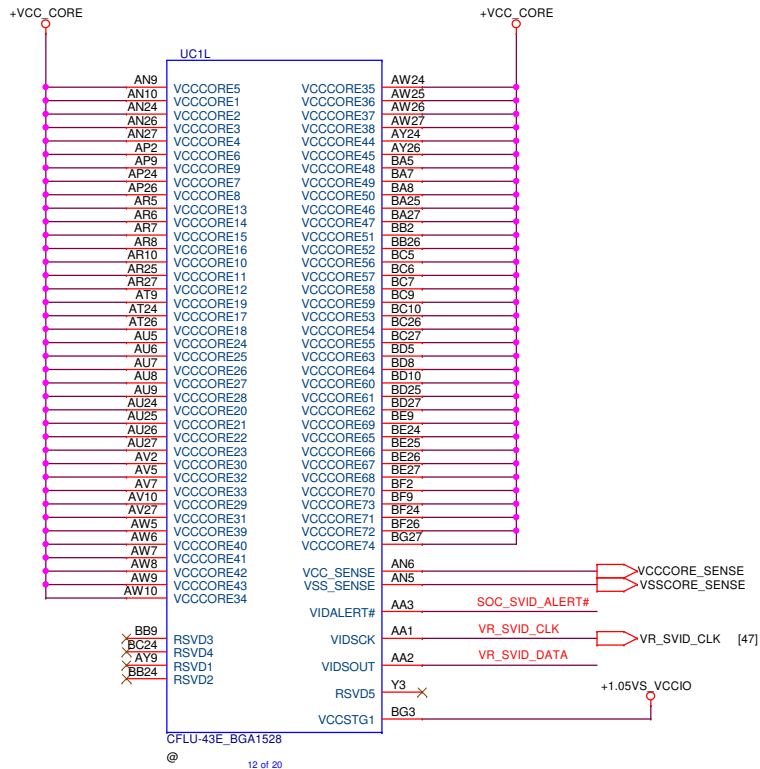
change package of 1U from 0201 to 0402

BSC Side

PSC Side

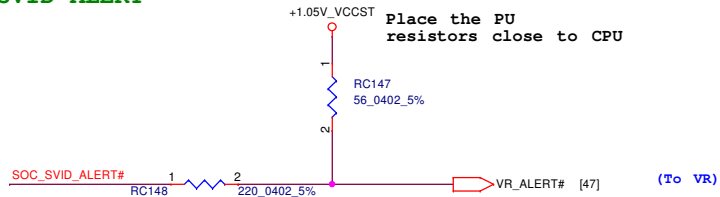


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Size	Document Number	Rev		0.2	
Custom	LA-H081P	Date		Monday, October 22, 2018	
Sheet		13		of 53	

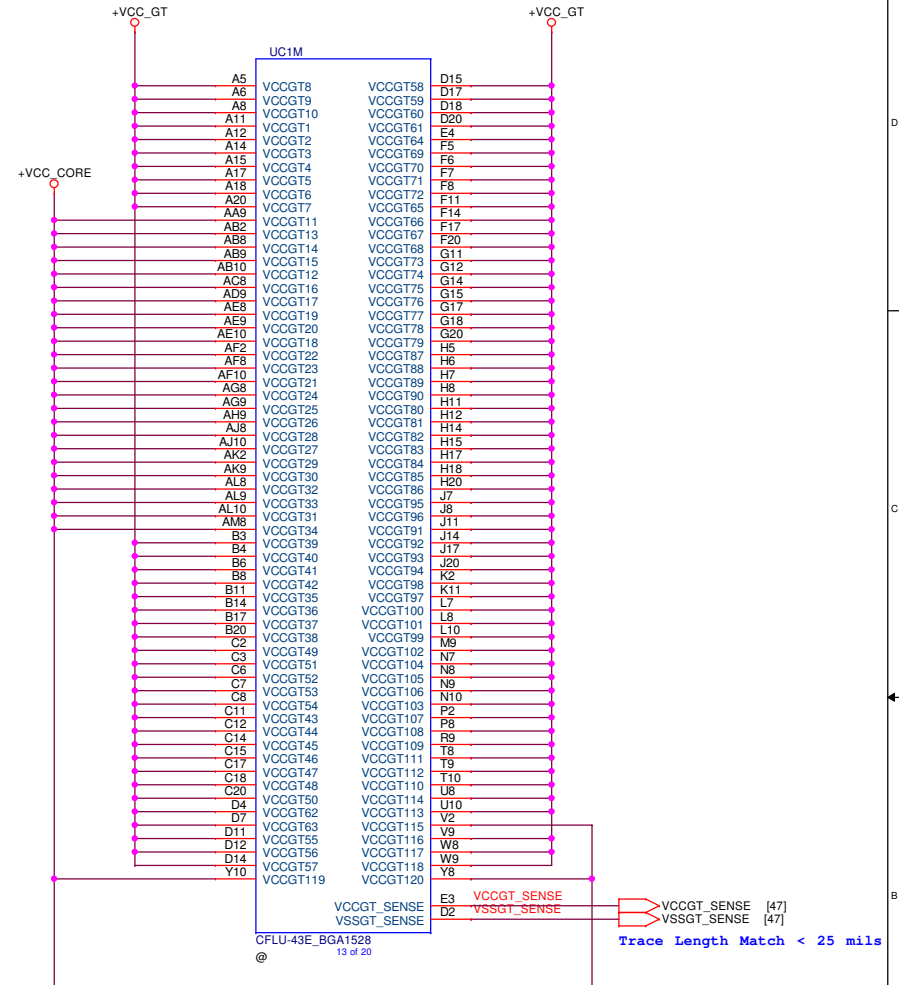
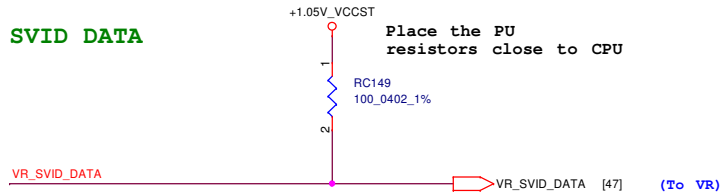


Trace Length Match < 25 mils

SVID ALERT



SVID DATA



Trace Length Match < 25 mils

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						Size		Document Number		Rev	
						Custom		LA-H081P		0.2	
						Date:		Monday, October 22, 2018		Sheet 15 of 53	

UC1R			
CR34	VSS_1	VSS_73	BL7
BT5	VSS_2	VSS_74	AE25
BY5	VSS_3	VSS_75	BM35
CP35	VSS_4	VSS_76	CM5
CM37	VSS_5	VSS_77	AE27
CK37	VSS_6	VSS_78	BM35
AW1	VSS_7	VSS_79	CM9
CM1	VSS_8	VSS_80	AE30
BD6	VSS_9	VSS_81	BM36
AY4	VSS_10	VSS_82	CM13
B34	VSS_11	VSS_83	AE7
E35	VSS_12	VSS_84	BM9
A4	VSS_13	VSS_85	CM17
AE24	VSS_14	VSS_86	AF27
AE26	VSS_15	VSS_87	BN30
AF25	VSS_16	VSS_88	CM21
AG24	VSS_17	VSS_89	AF3
AG26	VSS_18	VSS_90	BN7
AH24	VSS_19	VSS_91	CM25
AH25	VSS_20	VSS_92	AF30
B2	VSS_21	VSS_93	CM29
B36	VSS_22	VSS_94	AF33
C36	VSS_23	VSS_95	BP15
C37	VSS_24	VSS_96	AF36
CN1	VSS_25	VSS_97	AF4
CN2	VSS_26	VSS_98	CM5
CN37	VSS_27	VSS_99	AF7
CP2	VSS_28	VSS_100	BP25
D1	VSS_29	VSS_101	CM6
A32	VSS_30	VSS_102	AG10
F33	VSS_31	VSS_103	BP3
A3	VSS_32	VSS_104	CP1
BJ7	VSS_33	VSS_105	BP32
CJ36	VSS_34	VSS_106	CP11
A36	VSS_35	VSS_107	AH27
BK10	VSS_36	VSS_108	BP33
CJ4	VSS_37	VSS_109	CP13
AB27	VSS_38	VSS_110	AH28
BK2	VSS_39	VSS_111	BP4
CK1	VSS_40	VSS_112	CP15
AB3	VSS_41	VSS_113	AH29
BK28	VSS_42	VSS_114	BP7
AB30	VSS_43	VSS_115	CP19
BK3	VSS_44	VSS_116	AH30
CK4	VSS_45	VSS_117	CP21
AB33	VSS_46	VSS_118	AH31
BK33	VSS_47	VSS_119	BR19
CK7	VSS_48	VSS_120	CP27
AB36	VSS_49	VSS_121	AH33
BK4	VSS_50	VSS_122	BR25
CL2	VSS_51	VSS_123	AH35
AB4	VSS_52	VSS_124	CP37
BK7	VSS_53	VSS_125	AJ25
CM13	VSS_54	VSS_126	BT15
AB7	VSS_55	VSS_127	AJ28
BL25	VSS_56	VSS_128	BT16
CM17	VSS_57	VSS_129	CP9
AC10	VSS_58	VSS_130	AJ7
BL28	VSS_59	VSS_131	CR2
CM21	VSS_60	VSS_132	AK3
AC27	VSS_61	VSS_133	CR36
BL29	VSS_62	VSS_134	AK33
CM25	VSS_63	VSS_135	D21
AC30	VSS_64	VSS_136	AK36
BL30	VSS_65	VSS_137	BT25
CM29	VSS_66	VSS_138	D25
BL31	VSS_67	VSS_139	AK4
AD33	VSS_68	VSS_140	BT28
BL32	VSS_69	VSS_141	BT33
CM33	VSS_70	VSS_142	D5
AD35	VSS_71	VSS_143	AL29
	VSS_72	VSS_144	

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UC1S			
BT35	VSS_145	VSS_217	BY25
D6	VSS_146	VSS_218	J18
AL32	VSS_147	VSS_219	AU32
BT36	VSS_148	VSS_220	BY28
D8	VSS_149	VSS_221	J21
AL7	VSS_150	VSS_222	AV25
D9	VSS_151	VSS_223	BY33
AM10	VSS_152	VSS_224	J24
BU11	VSS_153	VSS_225	AV28
E23	VSS_154	VSS_226	BY35
AM28	VSS_155	VSS_227	J33
E27	VSS_156	VSS_228	AV3
AM33	VSS_157	VSS_229	BY36
BU23	VSS_158	VSS_230	J36
E29	VSS_159	VSS_231	AV33
AM35	VSS_160	VSS_232	J6
BU24	VSS_161	VSS_233	AV36
E31	VSS_162	VSS_234	C1
BU25	VSS_163	VSS_235	K21
E33	VSS_164	VSS_236	AV4
AN25	VSS_165	VSS_237	C21
BU7	VSS_166	VSS_238	K22
E9	VSS_167	VSS_239	AV6
AN28	VSS_168	VSS_240	C25
BV11	VSS_169	VSS_241	K24
F12	VSS_170	VSS_242	AV8
AN29	VSS_171	VSS_243	C29
F15	VSS_172	VSS_244	K25
AN30	VSS_173	VSS_245	AW28
F18	VSS_174	VSS_246	C33
AN31	VSS_175	VSS_247	K27
BV3	VSS_176	VSS_248	AW29
F2	VSS_177	VSS_249	C4
AN7	VSS_178	VSS_250	K28
BV31	VSS_179	VSS_251	AW3
F21	VSS_180	VSS_252	C9
AN8	VSS_181	VSS_253	K29
BV33	VSS_182	VSS_254	AW30
F24	VSS_183	VSS_255	CA11
BV4	VSS_184	VSS_256	K3
F3	VSS_185	VSS_257	AW31
AP3	VSS_186	VSS_258	CA15
BW11	VSS_187	VSS_259	K30
F4	VSS_188	VSS_260	AY33
AP33	VSS_189	VSS_261	CA22
BW15	VSS_190	VSS_262	K31
G21	VSS_191	VSS_263	AY35
AP36	VSS_192	VSS_264	B12
G27	VSS_193	VSS_265	K4
AP4	VSS_194	VSS_266	B15
G33	VSS_195	VSS_267	CA25
AR28	VSS_196	VSS_268	K9
G35	VSS_197	VSS_269	B18
G36	VSS_198	VSS_270	CB11
AT33	VSS_199	VSS_271	L27
BW24	VSS_200	VSS_272	B21
G9	VSS_201	VSS_273	L33
AT35	VSS_202	VSS_274	B23
H21	VSS_203	VSS_275	L35
AT36	VSS_204	VSS_276	B25
BW7	VSS_205	VSS_277	CB18
H27	VSS_206	VSS_278	L36
AT4	VSS_207	VSS_279	B27
BY11	VSS_208	VSS_280	CB19
AU10	VSS_209	VSS_281	L6
BY15	VSS_210	VSS_282	B29
H9	VSS_211	VSS_283	CB2
AU28	VSS_212	VSS_284	N25
BY22	VSS_213	VSS_285	CB20
B31	VSS_214	VSS_286	N27
AU29	VSS_215	VSS_287	CB25
J15	VSS_216	VSS_288	
		VSS_289	

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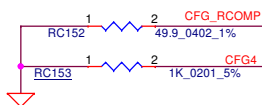
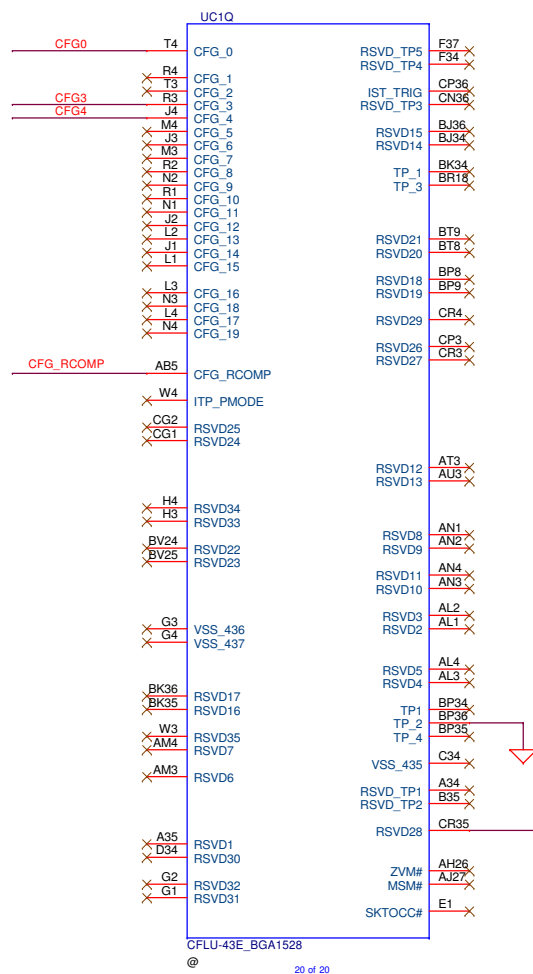
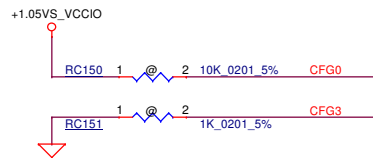
@ 18 of 20

UC1T			
N6	VSS_290	VSS_362	CF23
B37	VSS_291	VSS_363	V4
CB3	VSS_292	VSS_364	BE30
P10	VSS_293	VSS_365	CF28
B5	VSS_294	VSS_366	W10
CB33	VSS_295	VSS_367	BE31
P3	VSS_296	VSS_368	CF3
B7	VSS_297	VSS_369	W27
CB4	VSS_298	VSS_370	CF4
P33	VSS_299	VSS_371	BF3
B9	VSS_300	VSS_372	CG33
CB7	VSS_301	VSS_373	W7
P36	VSS_302	VSS_374	BF33
BA10	VSS_303	VSS_375	CG7
CG11	VSS_304	VSS_376	BF36
P4	VSS_305	VSS_377	Y26
BA28	VSS_306	VSS_378	BF4
P7	VSS_307	VSS_379	CH31
BA3	VSS_308	VSS_380	Y27
CC20	VSS_309	VSS_381	BG25
R27	VSS_310	VSS_382	Y30
BB3	VSS_311	VSS_383	BG28
CC25	VSS_312	VSS_384	CJ11
R28	VSS_313	VSS_385	Y33
BB33	VSS_314	VSS_386	CJ14
CC28	VSS_315	VSS_387	Y35
R29	VSS_316	VSS_388	BH28
BB36	VSS_317	VSS_389	CJ19
CC31	VSS_318	VSS_390	Y7
R30	VSS_319	VSS_391	BH29
BB4	VSS_320	VSS_392	CJ23
CC7	VSS_321	VSS_393	BH32
R31	VSS_322	VSS_394	CJ28
BC25	VSS_323	VSS_395	BH33
CD11	VSS_324	VSS_396	CJ33
T27	VSS_325	VSS_397	BH35
CD12	VSS_326	VSS_398	CJ35
T30	VSS_327	VSS_399	BP19
BC29	VSS_328	VSS_400	BR16
CD14	VSS_329	VSS_401	BY19
T33	VSS_330	VSS_402	CC16
T35	VSS_331	VSS_403	BU16
BC32	VSS_332	VSS_404	CC14
CD24	VSS_333	VSS_405	BR22
T36	VSS_334	VSS_406	BU20
CD25	VSS_335	VSS_407	CD20
T7	VSS_336	VSS_408	BT14
BC8	VSS_337	VSS_409	BP12
CE33	VSS_338	VSS_410	CB24
U26	VSS_339	VSS_411	CC24
BD28	VSS_340	VSS_412	J5
CE35	VSS_341	VSS_413	U24
U7	VSS_342	VSS_414	BD7
BD33	VSS_343	VSS_415	AR4
CE36	VSS_344	VSS_416	AU4
V26	VSS_345	VSS_417	AW4
BD35	VSS_346	VSS_418	BA6
CE7	VSS_347	VSS_419	BC4
V27	VSS_348	VSS_420	BE4
BD36	VSS_349	VSS_421	BE5
CF11	VSS_350	VSS_422	BA4
V3	VSS_351	VSS_423	BD4
BE10	VSS_352	VSS_424	BG4
CF14	VSS_353	VSS_425	CJ2
V30	VSS_354	VSS_426	CJ3
BE28	VSS_355	VSS_427	AM5
CF19	VSS_356	VSS_428	CM4
V33	VSS_357	VSS_429	AC5
BE29	VSS_358	VSS_430	AC5
CF2	VSS_359	VSS_431	AC5
V36	VSS_360	VSS_432	CR6
BE3	VSS_361	VSS_433	

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						Size		Document Number		Rev	
						Custom		LA-H081P		0.2	
						Date:		Monday, October 22, 2018		Sheet	
										16 of 53	

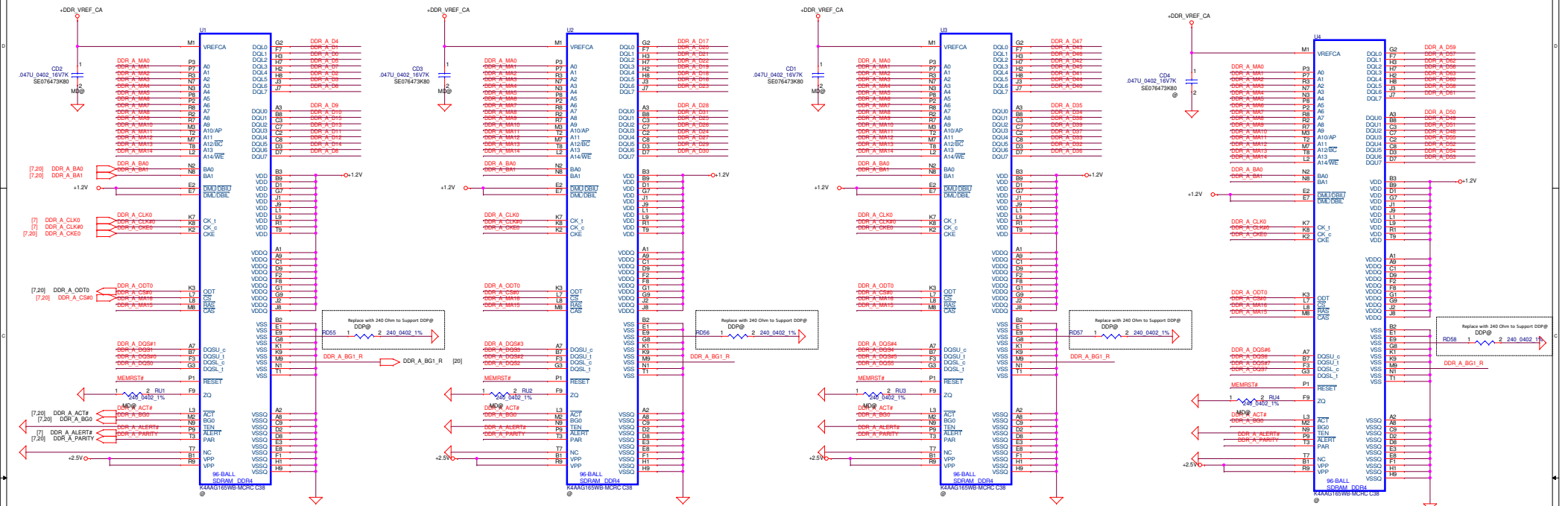


RSVD28 TP@ T2407 Follow Intel suggestion reserve TP

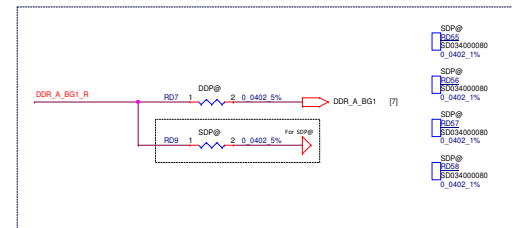
DFX Privacy Strap	
CFG3	<p>1 : Disabled; Set DFX disable bit in debug interface MSR</p> <p>0 : Enabled; Set DFX enable bit in debug interface MSR</p>
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port at tachedt o E mbedded Dsplay port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

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				Date:	Monday, October 22, 2018
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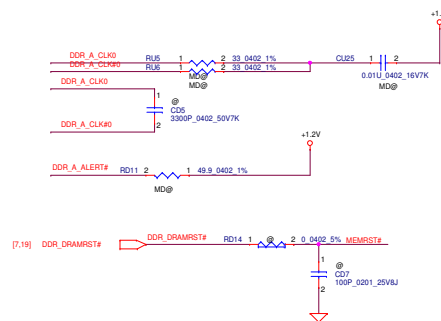
Interleaved Memory



Co-lay for SDP / DDP Memory DIE



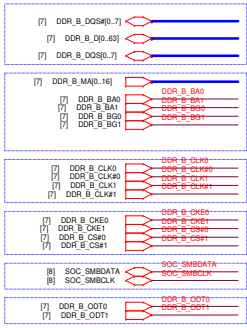
CLOCK TERMINATION



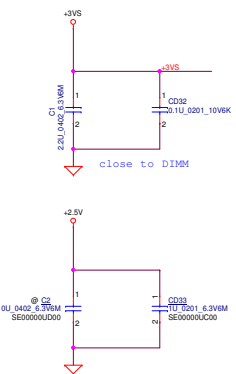
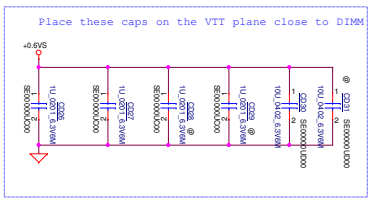
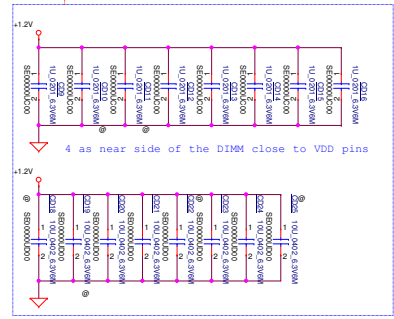
On Board RAM - Data Mapping

U4	DQ	U2	DQ	U3	DQ	U1	DQ
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

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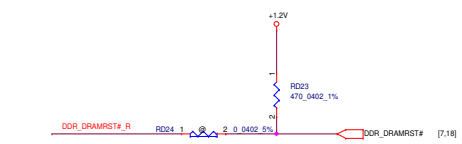
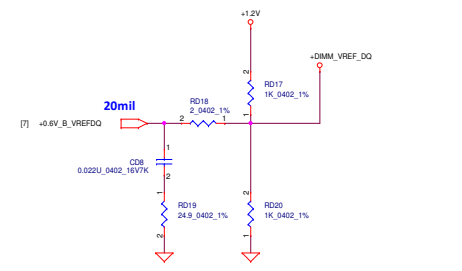


Layout Note: Check voltage tolerance of VREF_DQ at the DIMM socket

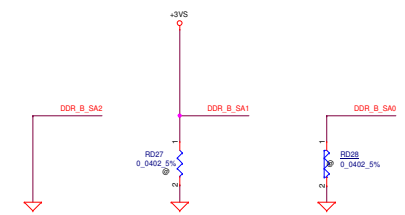


Reverse Type

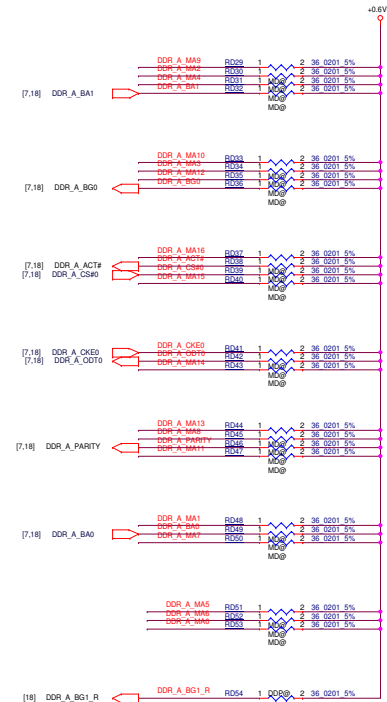
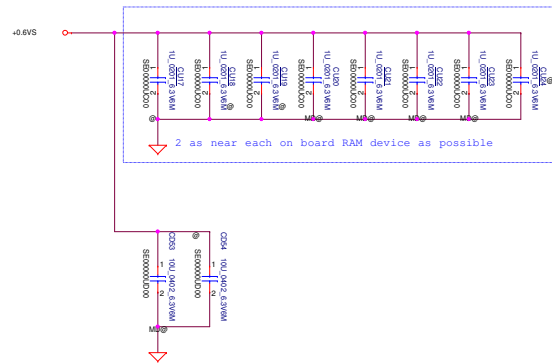
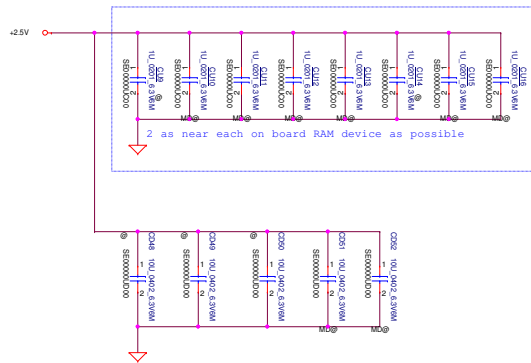
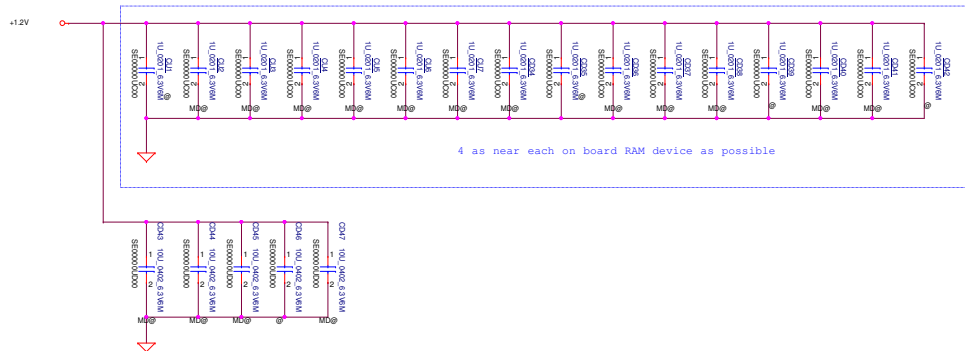
2-3A to 1 DIMMs/channel



JDIMM1 ADDRESS (PLACE CLOSE TO DIMM)

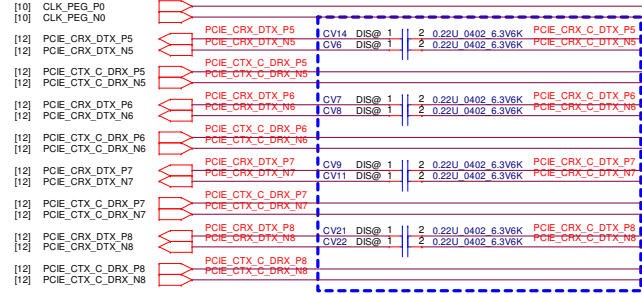


[7.18] DDR_A_MAP.146

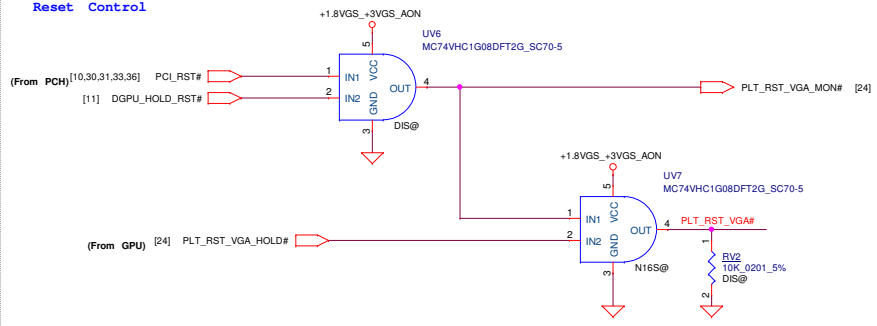


PCIE CLK

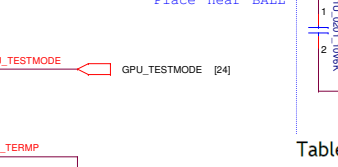
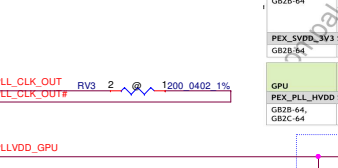
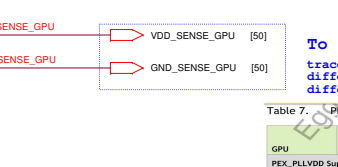
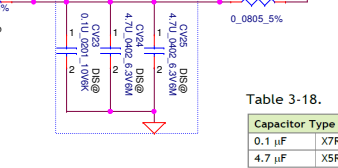
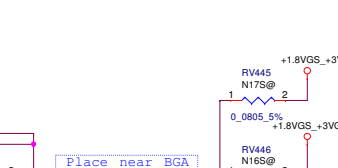
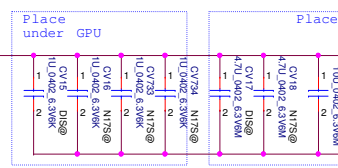
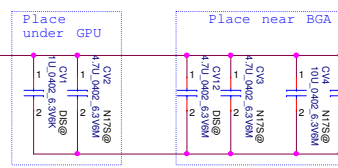
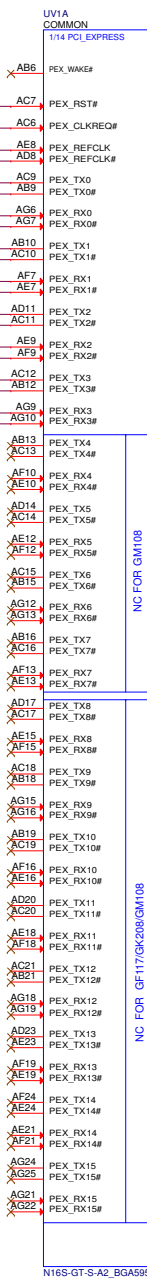
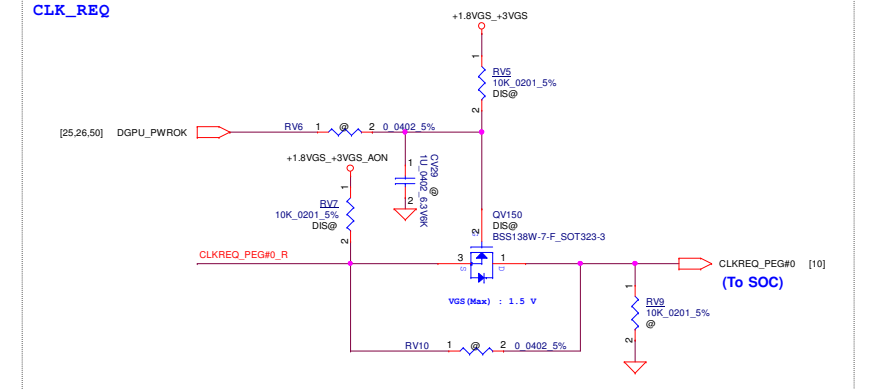
PCIE X4 Bus



Reset Control



CLK_REQ



GPU Package Type	Capacitor Type	Footprint	Population	Location
GR28-64	1.0 µF X65	0402	1	Under GPU
GR28-64	4.7 µF X65	0603	1	Near GPU
GR28-64	10 µF X5R	0805	1	Midway between GPU and Power Supply
GR28-64	22 µF X5R	0805	1	Midway between GPU and Power Supply

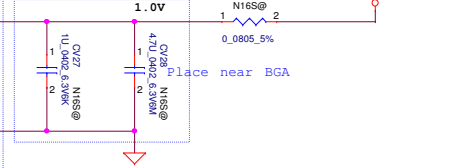
GPU	Capacitor Type	Footprint	Population	Location
N16 PEX_I0VDD (N17 PEX_DVDD) Supply Rail				
GR28-64, GR28-64	1.0 µF X65	0402	1	Under GPU
GR28-64, GR28-64	4.7 µF X65	0603	1	Under GPU
GR28-64, GR28-64	4.7 µF X65	0603	1	Near GPU
GR28-64, GR28-64	10 µF X65	0805	2	Midway between GPU and Power Supply
GR28-64, GR28-64	22 µF X65	0805	0	Midway between GPU and Power Supply
N16 PEX_I0VDD (N17 PEX_HVDD) Supply Rail				
GR28-64, GR28-64	1.0 µF X65	0402	1	Under GPU
GR28-64, GR28-64	4.7 µF X65	0603	1	Near GPU
GR28-64, GR28-64	10 µF X65	0805LP	1	Midway between GPU and Power Supply
GR28-64, GR28-64	22 µF X65	0805LP	1	Midway between GPU and Power Supply

Capacitor Type	Footprint	Population	Location
0.1 µF X7R	0402	1	Near GPU
4.7 µF X5R	0603	2	Near GPU

Capacitor Type	Footprint	Population	Location
0.1 µF X7R	0402	1	Near GPU
4.7 µF X5R	0603	2	Near GPU

GPU	Capacitor Type	Footprint	Population	Location
PEX_PLLVDD Supply Rail				
GR28-64	0.1 µF X7R	0402	1	Under GPU
GR28-64	1.0 µF X5R	0603	1	Near GPU
GR28-64	4.7 µF X5R	0805	1	Near GPU
PEX_SVDD_3V3 Supply Rail				
GR28-64	4.7 µF X5R	0603	2	Near GPU

GPU	Capacitor Type	Footprint	Population	Location
PEX_PLLVDD Supply Rail				
GR28-64, GR28-64	0.1 µF X7R	0402	1	Near GPU



Capacitor Type	Footprint	Population	Location
0.1 µF X7R	0402	1	Under GPU
1.0 µF X5R	0603	1	Near GPU
4.7 µF X5R	0805	1	Near GPU

DAC_A

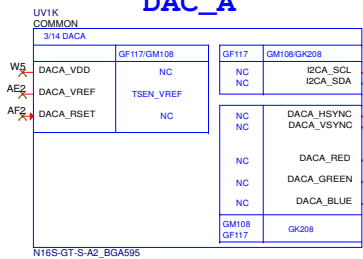
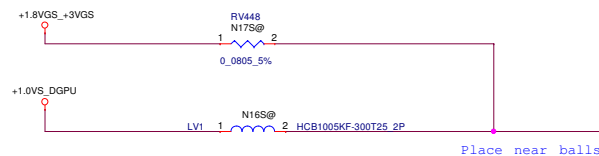


Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	N16	N17	Location
PLLVD (N17: KS_PLLVD) Supply Rail					
GB2B-64, GB2C-64	0.1 μ F X7R	0402	1	0	Under GPU
	22 μ F X5R	0805	1	0	Near GPU
Bead Type					
	L2=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVD and VID_PLLVD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 μ F X7R	0402	2	0	Under GPU
	10 μ F X5R	0603	0	0	Near GPU
	47 μ F X5R	0805	0	0	Near GPU
Bead Type					
	L2=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU



GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128	PLLVD	0.1 μ F	X7R 0402	1	Under GPU
		22 μ F	X5R 0805	1	Near GPU
Bead Type					
		30 Ω (ESR=0.05 Ω)	0402	1	Near GPU

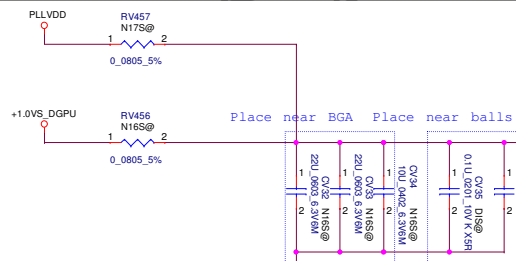
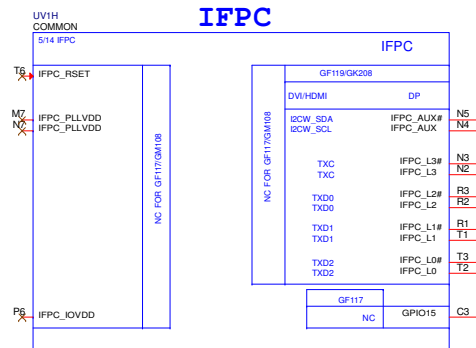


Table 3-33. SP_PLLVD Power Rail Filtering¹

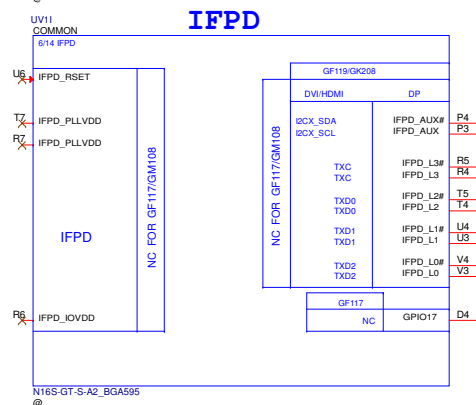
GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128, GB3B-256	SP_PLLVD (+VID_PLLVD) ¹	0.1 μ F	X7R 0402	1 per ball	Under GPU
		10 μ F	X5R 0603	1	Near GPU
		47 μ F	X5R 0805	1	Near GPU
Bead Type					
		300 Ω (ESR=0.2 Ω)	0603	1	Near GPU

Note:
1. SP_PLLVD and VID_PLLVD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 8024 x 768 with a 240 Hz refresh rate.

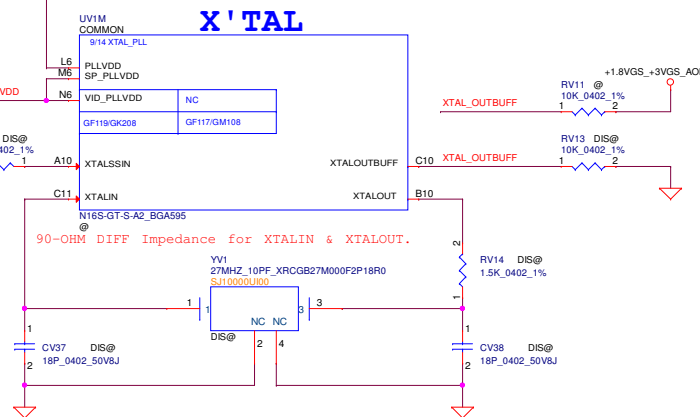
IFPC



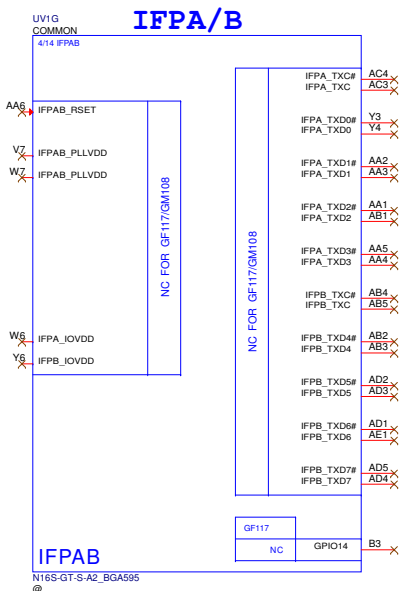
IFPD



X'TAL

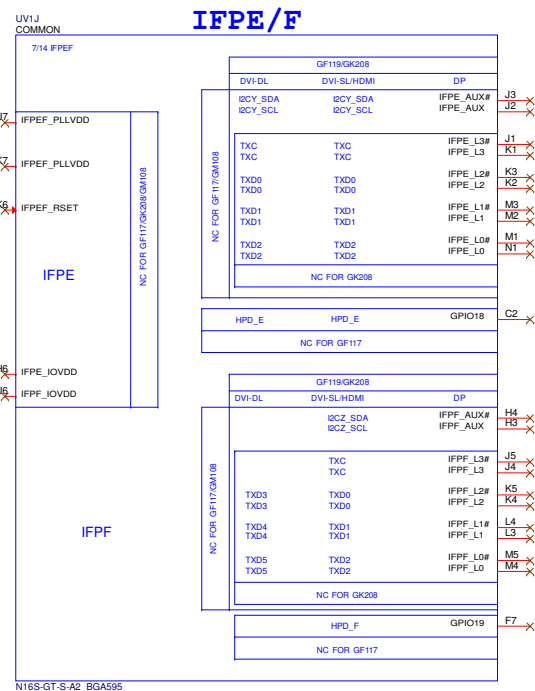


IFPA/B



IFPAB

IFPE/F



IFPF

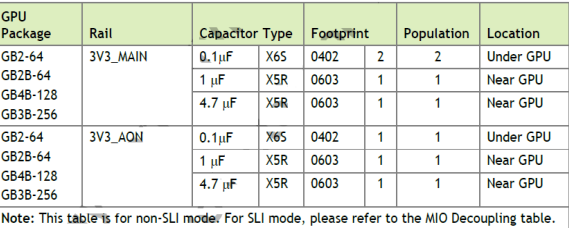
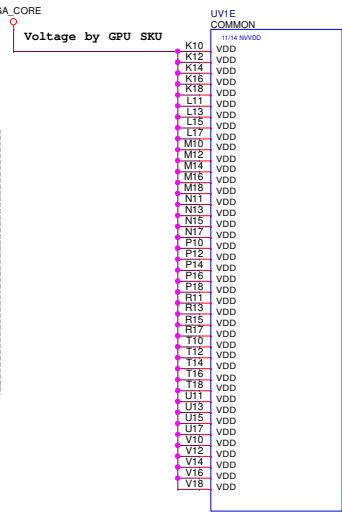
Security Classification	Compal Secret Data		Title	
Issued Date	2017/10/27	Deciphered Date	2019/04/09	Rev
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				0.2
LA-H081P				Monday, October 22, 2018
Sheet 22 of 53				



GPU	Capacitor Type	Population		
		Footprint	N16	N17 Location
FBVDD/Q Supply Rail for GDDR5				
G52B-64, G52C-64	0.1 μ F	X7R 0402	2	0 Under GPU
	1 μ F	X7R 0603	2	8 Under GPU
	4.7 μ F	X6S 0603	2	0 Under GPU
	10 μ F	X6S 0603	0	2 Under GPU
	10 μ F	X6S 0603	1	1 Near GPU
	22 μ F	X6S 0603W	1	3 Near GPU

Place near GPU

C1Z00 22uF x1 change to 10uF x2

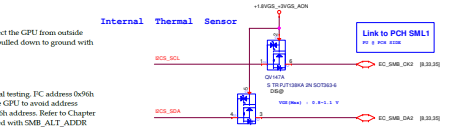
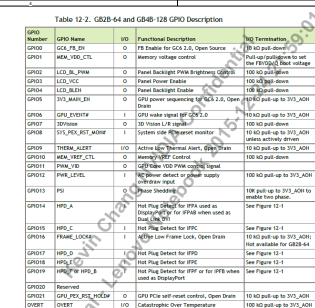


NC (N17: GPCPLL_AVDD) Supply Rail						
GB2C-64	0.1 μ F	X7R	0402	N/A	1	Under GPU
	4.7 μ F	X6S	0603	N/A	1	Near GPU
	22 μ F	X6S	0805	N/A	1	Near GPU
Bead Type						
	L=30 Ω (ESR=0.010 Ω)		0603	N/A	1	Near GPU

**** XPWR pins are configurable.**

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.



10.2.2 I²C Slave Address

The internal thermal sensor can be accessed through the FCS interface as described in the FC chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the FCS interface by the system is not supported. The default port address to access the internal thermal sensor over the FCS is 0x9E. Table 16-1 describes the byte-wise registers accessible through the FCS interface.

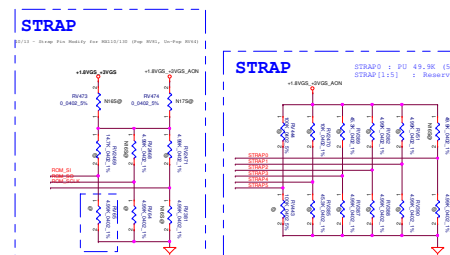










Table 2 χ^2 test results for the null hypothesis of no association between the variables

Item	Allowed	Item	Allowed	Item	Allowed
Item	Allowed	Item	Allowed	Item	Allowed










RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE
0x9 (LML) M2G	 0x000 N1T_H0G0 100K_0402.5%	 0x000 N1T_M0G0 100K_0402.5%  0x000 N1T_M0G0 100K_0402.5%	 0x000 N1T_M0G0 100K_0402.5%	
0xA (LMB) H2G	 0x000 N1T_H0G0 100K_0402.5%	 0x000 N1T_H0G0 100K_0402.5%  0x000 N1T_H0G0 100K_0402.5%	 0x000 N1T_H0G0 100K_0402.5%	

Strap Pins *see*

		U N17_H2G00		
		100K_0402_5%		

75 G1 VRAM Strap

Almond					
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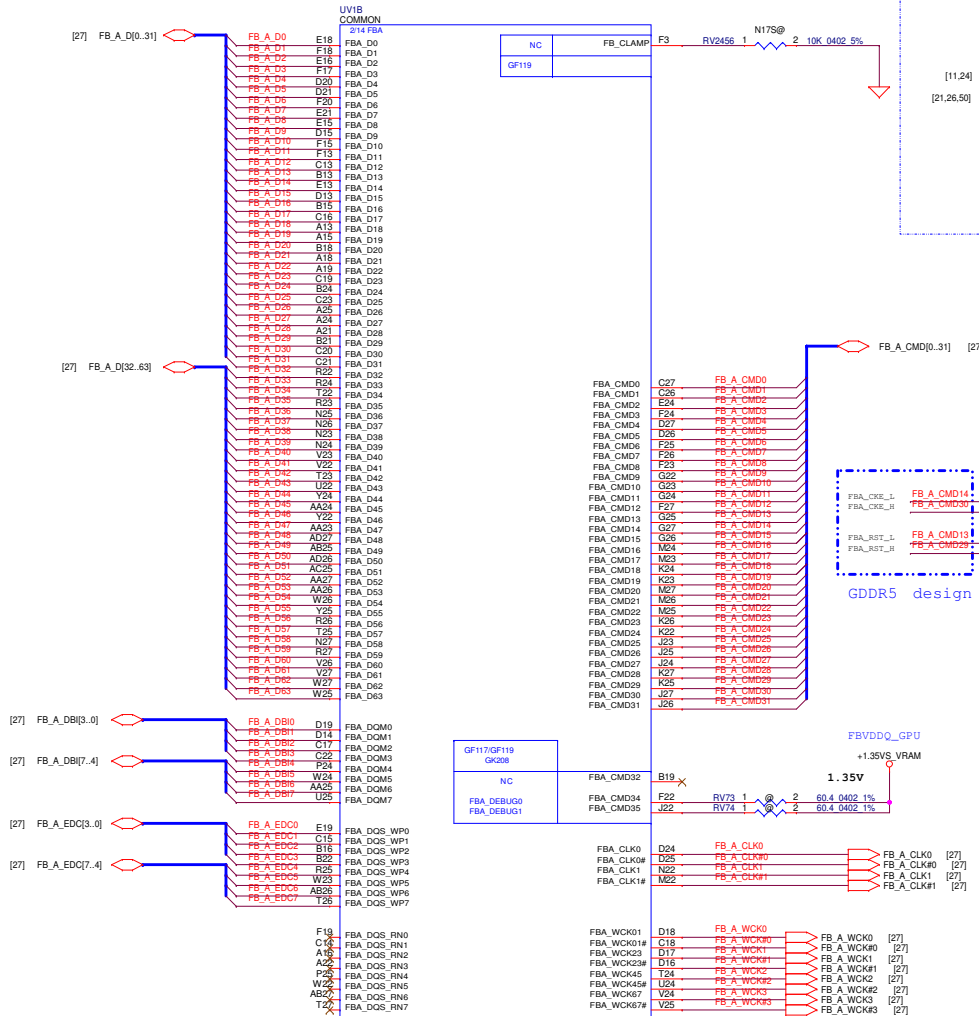
CFG	STRAP2	STRAP1	STRAP0	
(LL1) S2G	 01100 0	 01001 0	 01001 0	
(LL0)				
(LRL)				
(LRR)				
(RL1) M2G	 01000 0	 01001 0	 01001 0	
(RL0) R2G	 01000 0	 01000 0	 01004 0	
(RRL)				
(RRR)				
(LLL)				

1/3 Snap

Row Index	Strap Pins see Note			Resulting SORX_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
7	M	M	M	disabled	disabled	disabled	disabled
All other Strap Configurations				(Reserved)			

[illegible]

Co.	ps.	Note 1	Functions Selected by This Strapping
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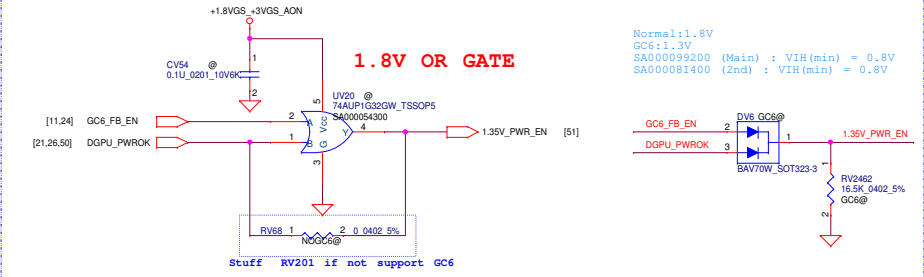


For VRAM DEBUG using
T2402 @ FB_VREF

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	N16	N17	Location
FB PLL Supply Rail for GDDR5						
GR2B-64, GR2B-64	0.1 μ F	X7R	0402	2	4	Under GPU
	22 μ F	X6S	0805	1	1	Near GPU
Bead Type						
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

For GC6



From DG-07158-001_v05_secured(NVDIA Spec)

7.1.8 CKE* Signal

Two copies of the clock enable signal (CKE*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE* signal requires a 10 k Ω pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

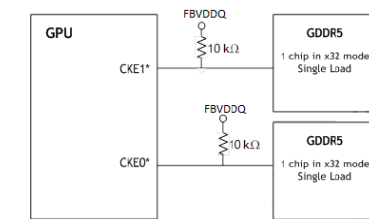


Figure 7-4. Clock Enable (CKE*) Signal Connection, $\times 32$ Mode

7.1.7.3 RST* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

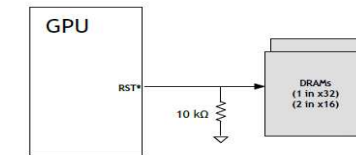
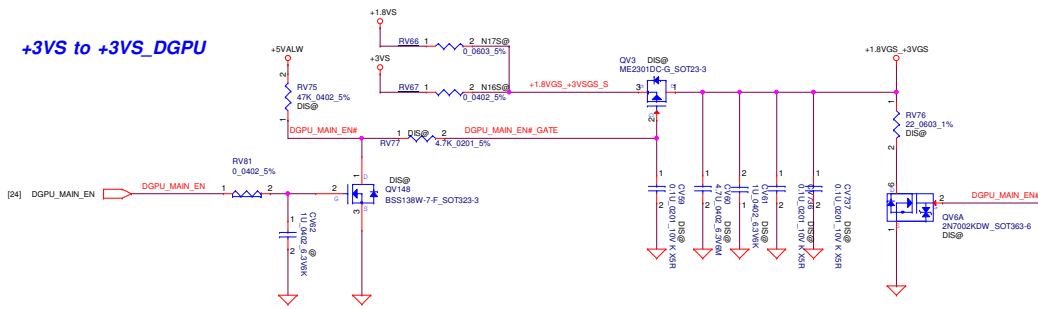


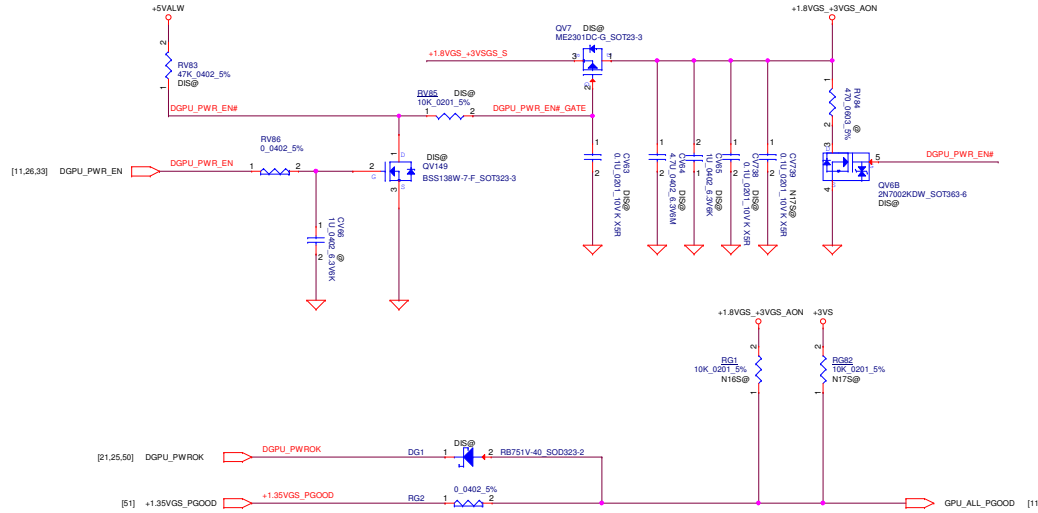
Figure 7-3. Reset Signal Connection

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GR2-64/ GR2B-64	FB_VREF and FB_VREF_AON Combined	0.1 μ F	X7R	0402	2
		22 μ F	X5R	0805	1
		Bead Type			
		30 Ω (ESR=0.010 Ω)		0603	1

+3VS to +3VS_DGPU



+3VS to +3VS_DGPU_AON



7.3.2.1 Power-Up Sequence

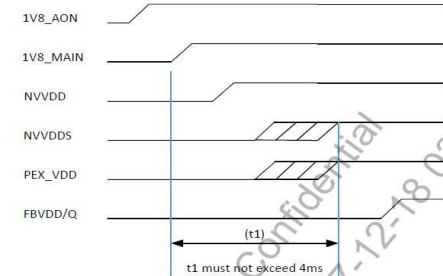
The following power-up sequence is required:

1V8_AON → 1V8_MAIN → NVVDD → NVVDDS / PEX_DVDD → FBVDD(Q)

► All GPU power rails must ramp up after 1V8_AON.

► FBVDD(Q) should ramp up after NVVDDS and PEX_DVDD.

All other 1.8V power rails can ramp up with 1V8_MAIN including PEX_HVDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX_DVDD.



re 7.5 Example of Power-Up Sequencing Order

7.3.2.2 Power-Down Sequence

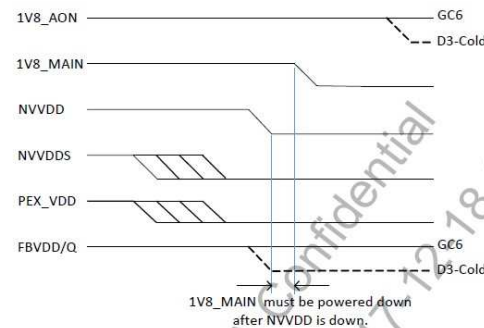


Table 7. Output EDP-Continuous

	NVVDD	GPU FBIO	FB Total ¹	1.0V Total ¹	1.8V Total ²
	—	1.35V ⁴	1.35V ⁴	1.0V ⁴	1.8V ⁴
Product	(A)	(A)	(A)	(A)	(A)
N17S-LG	15.4	2.5	5.0	0.1	0.2
N17S-G1	30.0	3.0	5.6	0.1	0.3
N17S-G0 ⁶	27.8	3.2	5.8	0.2	0.5
N17S-G2 ⁶	28.6	3.2	5.8	0.2	0.5

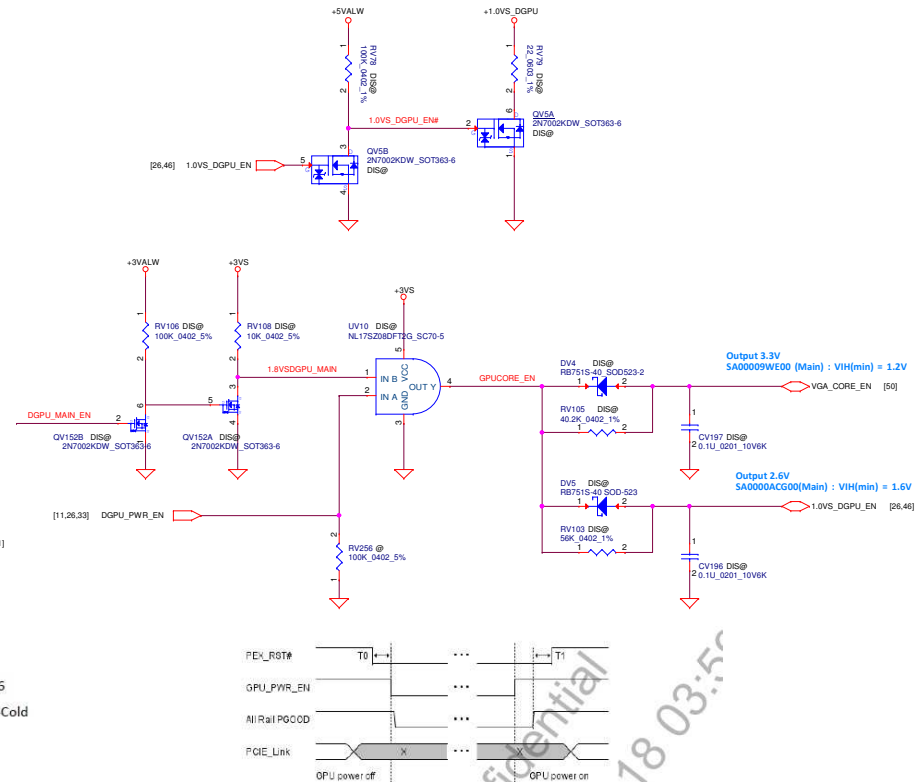


Figure 8.9 GC OFF Entry/Exit Timing Diagram

Table 8.1 GC OFF Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

VRAM Memory Partition A

Table 7-4. GDDR5 Mode H Mapping

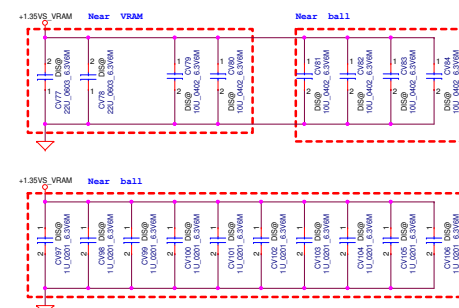
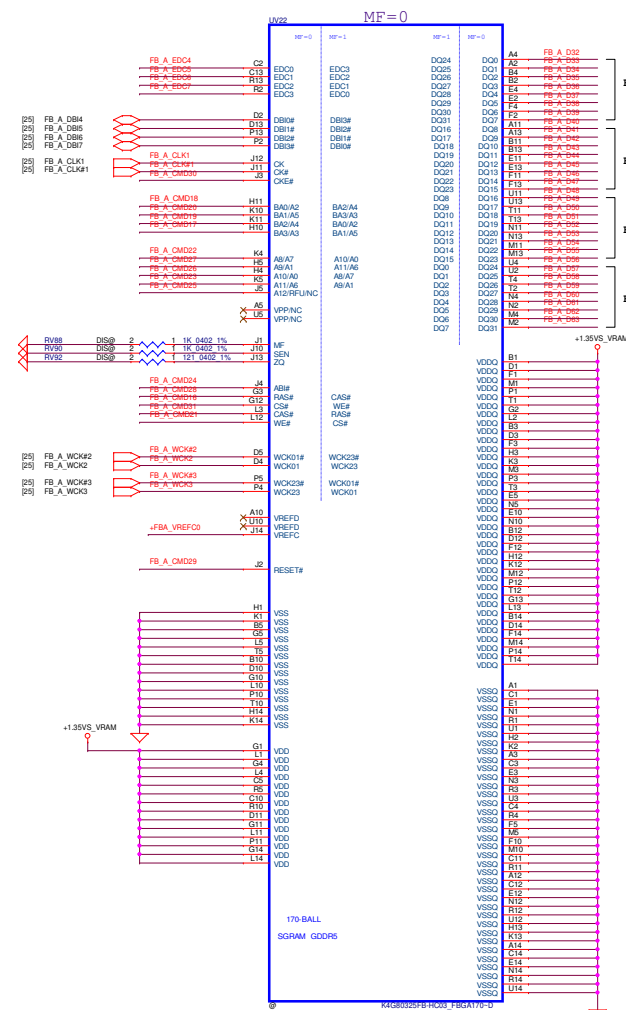
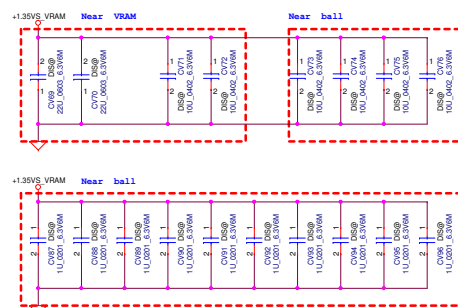
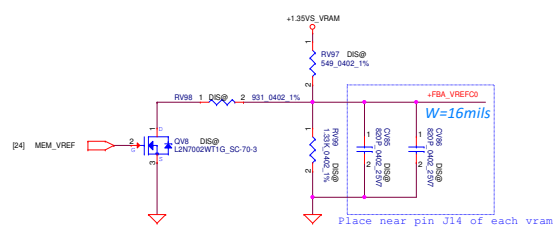
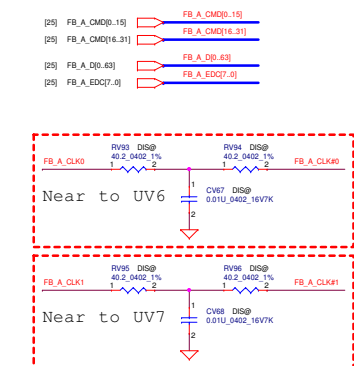
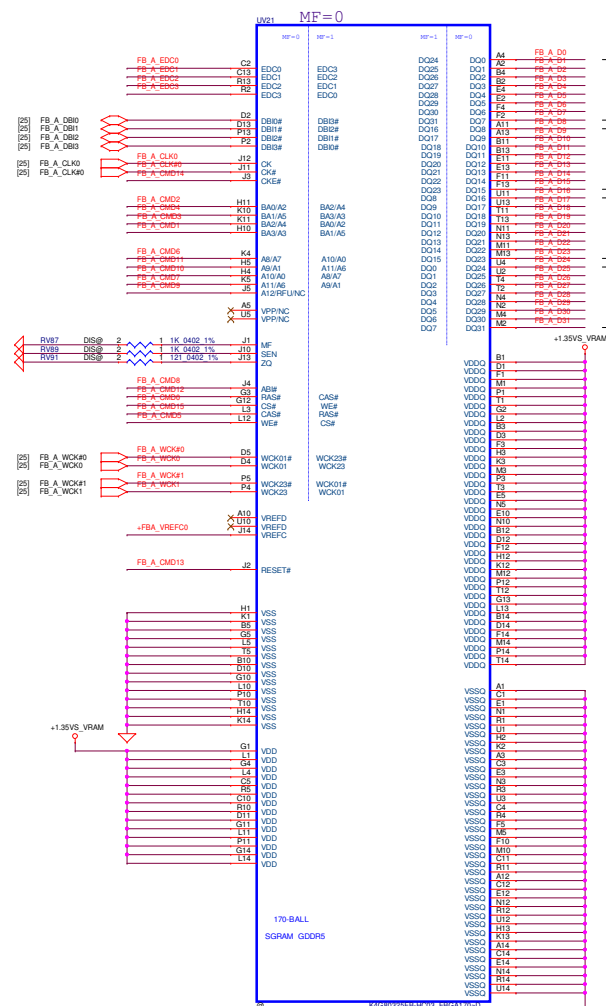
GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CM00	C5*	CM016	C5*
CM01	A3_BA3	CM017	A3_BA3
CM02	A2_BA0	CM018	A2_BA0
CM03	A4_BA2	CM019	A4_BA2
CM04	A5_BA1	CM020	A5_BA1
CM05	WE*	CM021	WE*
CM06	A7_AB	CM022	A7_AB
CM07	A6_A11	CM023	A6_A11
CM08	AB1*	CM024	AB1*
CM09	A12_RFU	CM025	A12_RFU
CM010	A0_A10	CM026	A0_A10
CM011	A1_A9	CM027	A1_A9
CM012	RA5*	CM028	RA5*
CM013	R5T*	CM029	R5T*
CM014	CKE*	CM030	CKE*
CM015	CAS*	CM031	CAS*
GB2-64, GB2B-64, GB4B-128 Channel 0 & 1			
CM032	Not_Used		
CM033 ¹	Not_Used		
CM034	DEBUG0 ¹		
CM035	DEBUG1 ¹		

Notes:

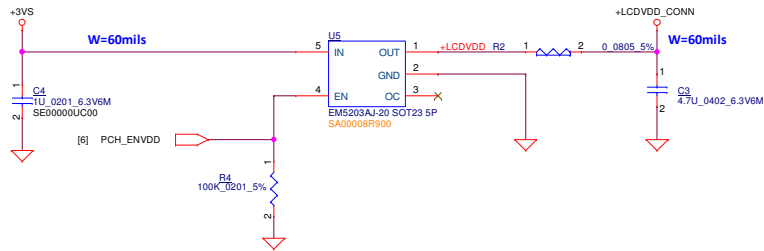
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to JRM-Mee section 7.1.13.

Notes:

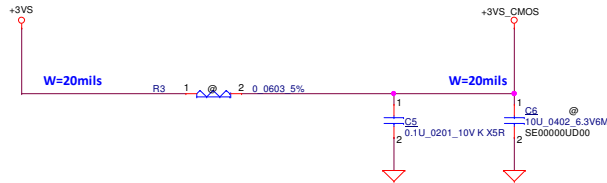
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to UKAM. See section 7.1.13.



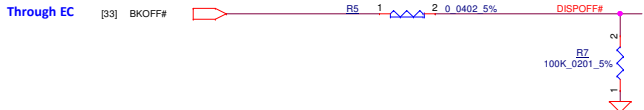
LCD POWER SWITCH



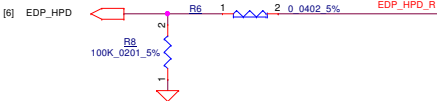
CAMERA POWER CIRCUIT



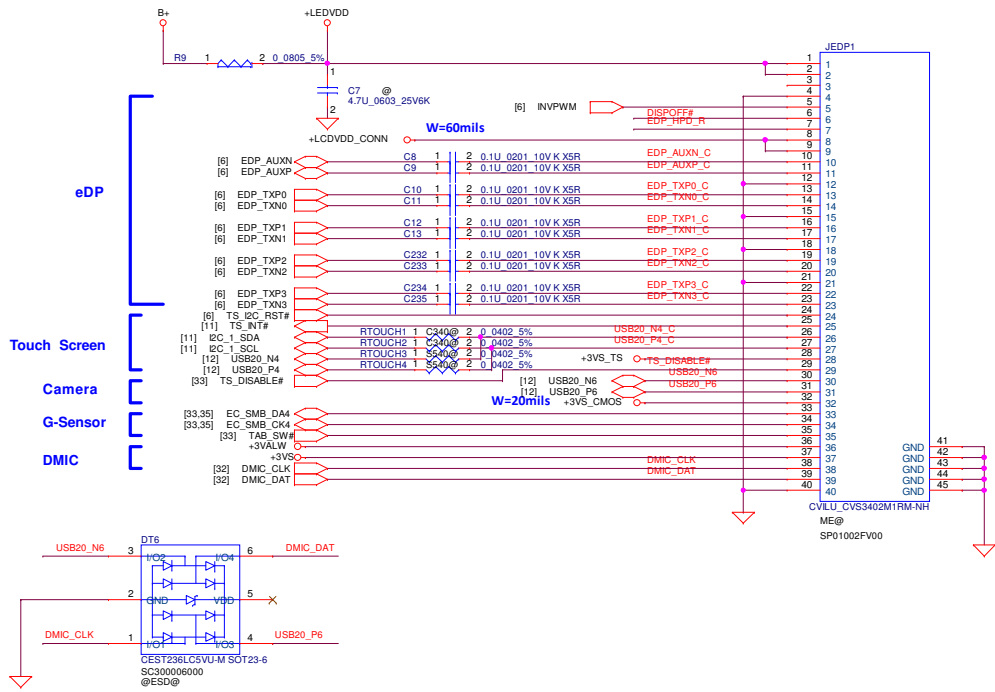
DISPLAY OFF



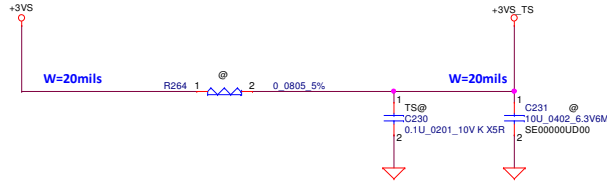
HOT PLUG DETECT



eDP CONNECTOR

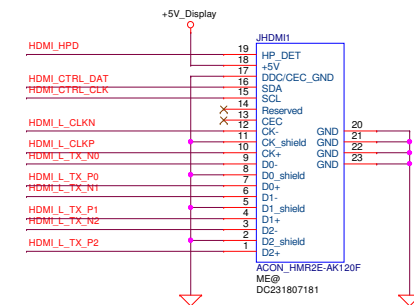
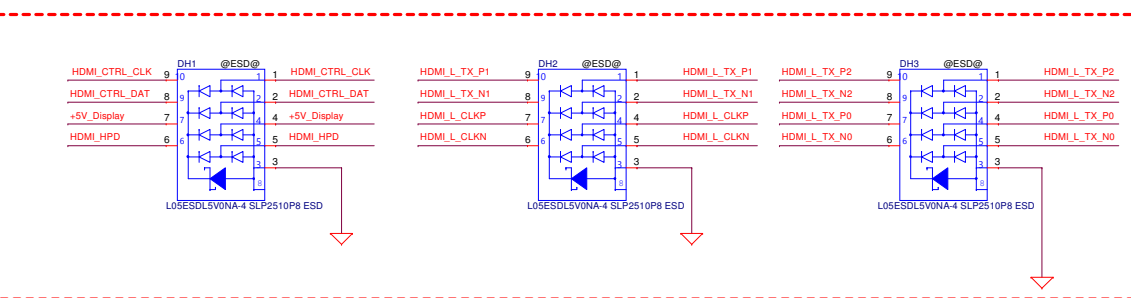
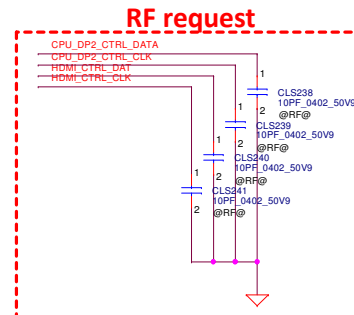
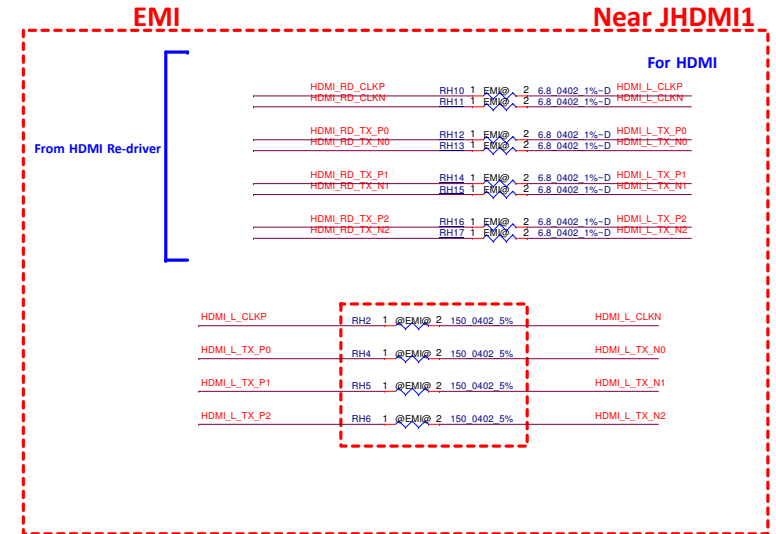
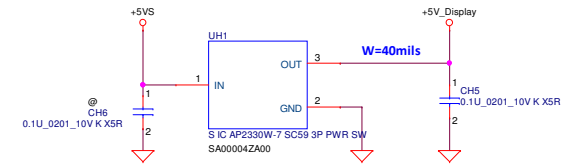
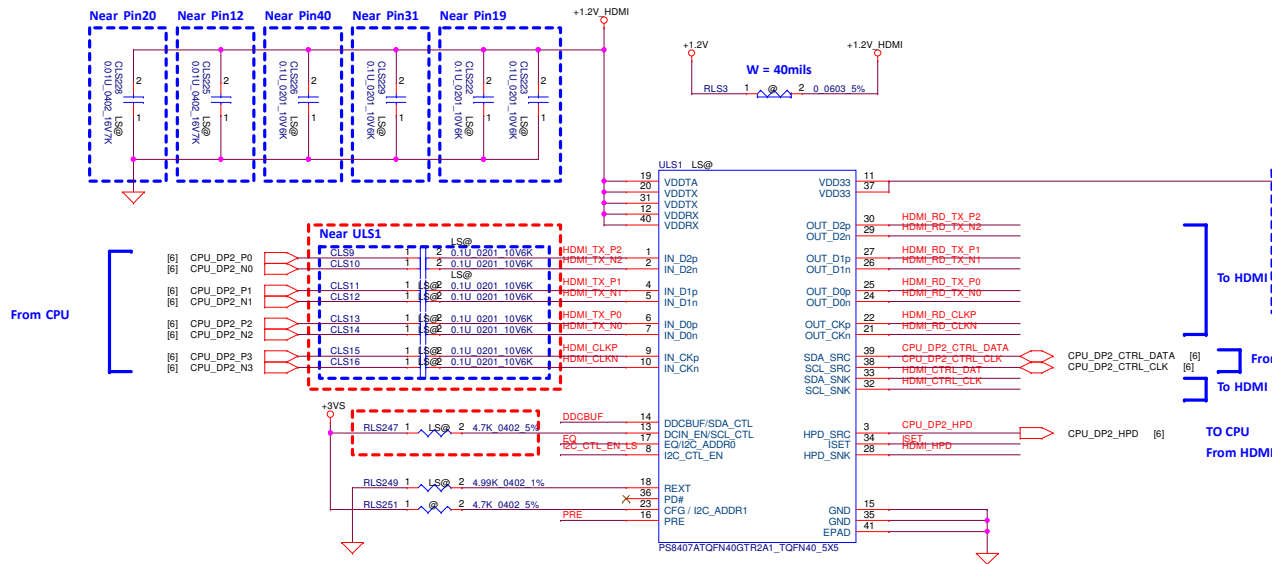


Touch Screen POWER CIRCUIT



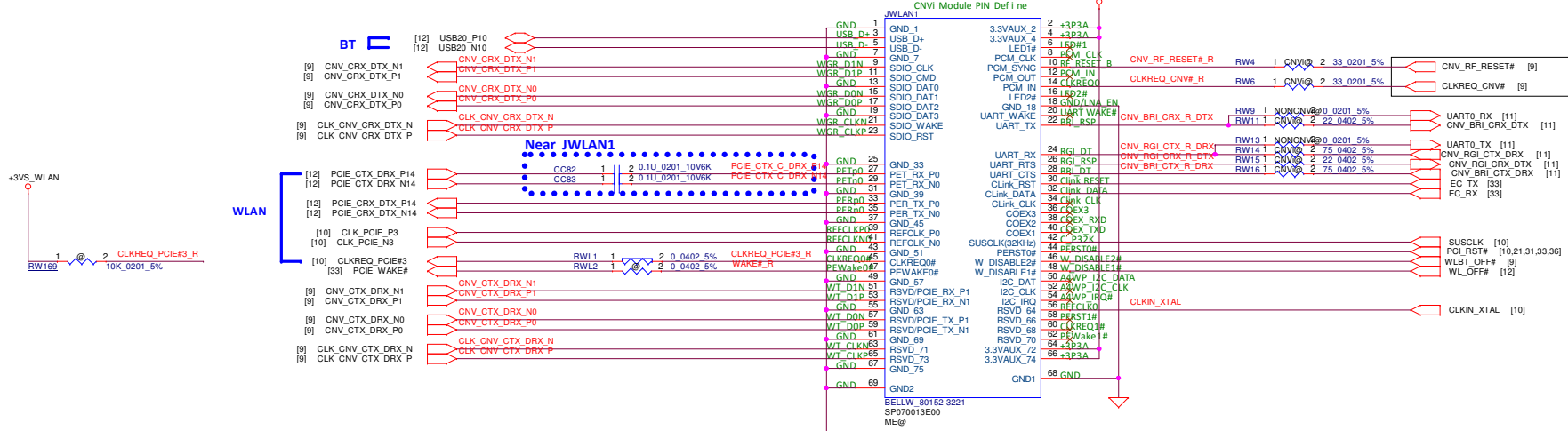
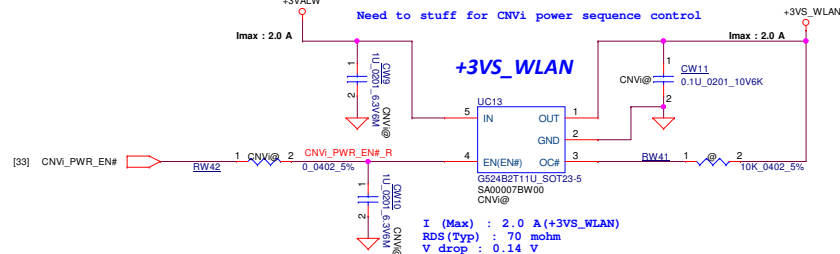
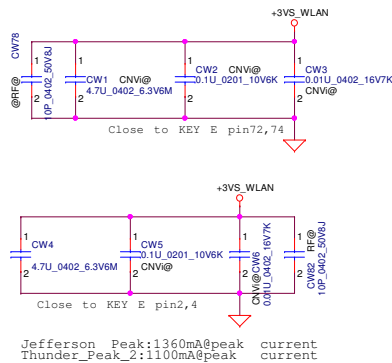
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Issued Date				2018/04/09				eDP / Camera / MIC			
Deciphered Date				2019/04/09				LA-H081P			
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Date:				Monday, October 22, 2018				0.2			
Sheet				28				of			
1				2				3			

HDMI



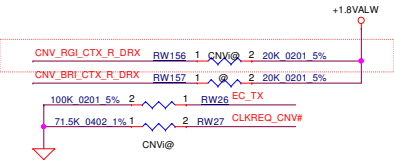
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Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	HDMI	
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				Custom	LA-H081P	0.2
Date: Monday, October 22, 2018				Sheet	29	of 53

NGFF WLAN /BT(Key E)



The connectivity module power supply pin shall be connected directly to thr rail DSW.
From
567240_Intel_Wireless_AC_9560_Jefferson_Peak_EPS_Rev1.1

PCH EDS : M.2 CNV Mode Select
GPP_F6/CNV_RGL_DT
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

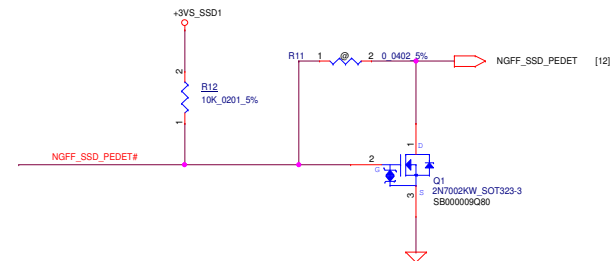
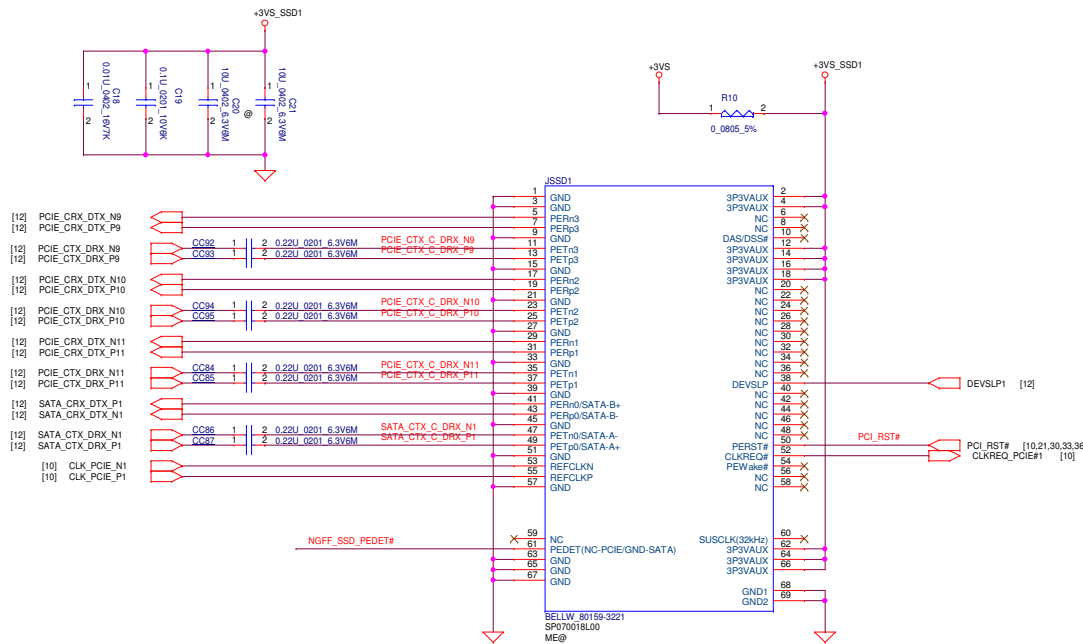


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Issued Date		2018/04/09		Deciphered Date	
2019/04/09		2019/04/09		Title	
2019/04/09		2019/04/09		NGFF WLAN / BT	
2019/04/09		2019/04/09		Size	
2019/04/09		2019/04/09		Document Number	
2019/04/09		2019/04/09		Rev	
2019/04/09		2019/04/09		0.2	
2019/04/09		2019/04/09		Date	
2019/04/09		2019/04/09		Monday, October 22, 2018	
2019/04/09		2019/04/09		Sheet	
2019/04/09		2019/04/09		30 of 53	

SSD(TYPE M)

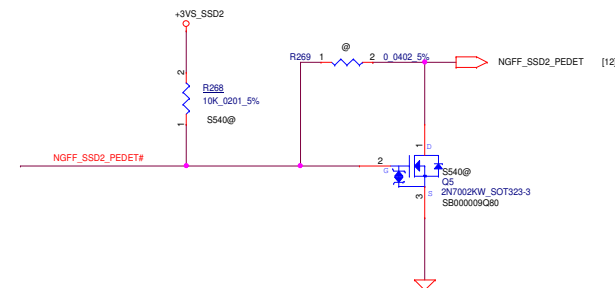
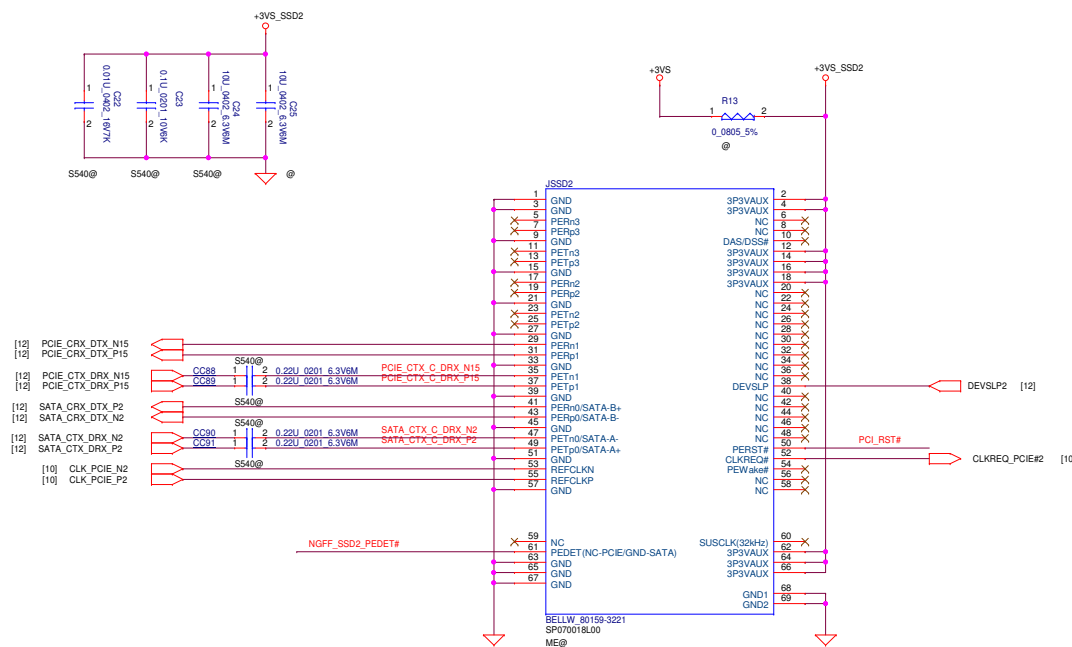
SSD PCIE

SSD SATA



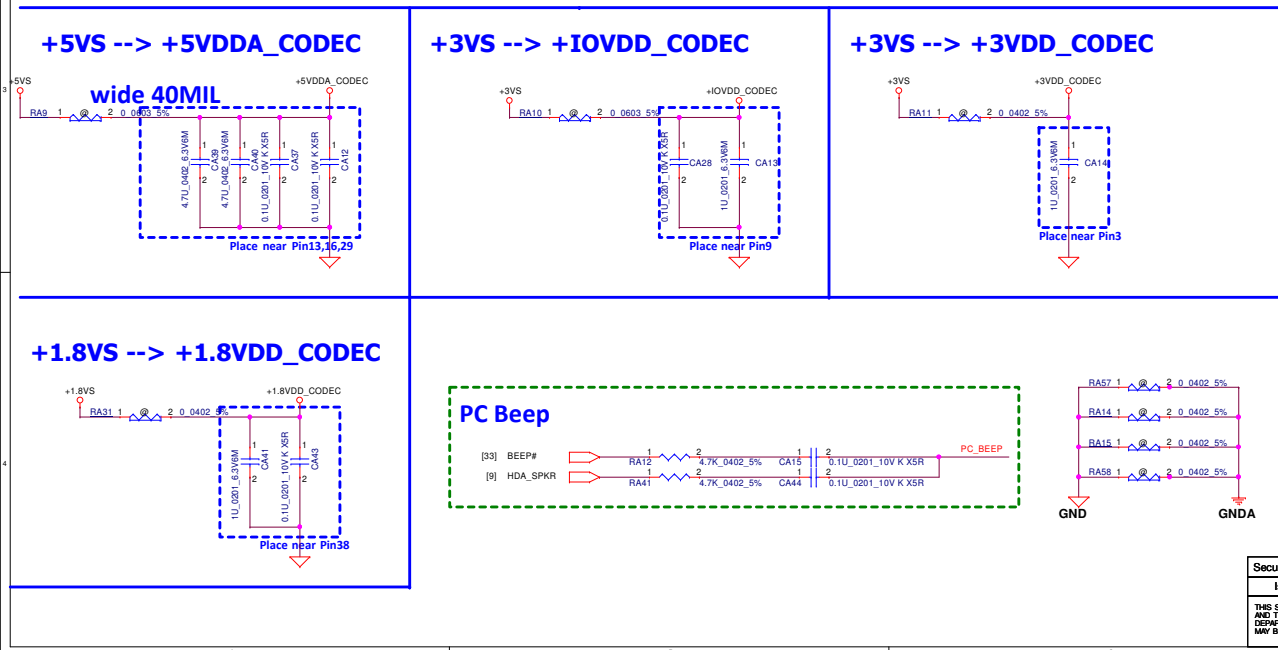
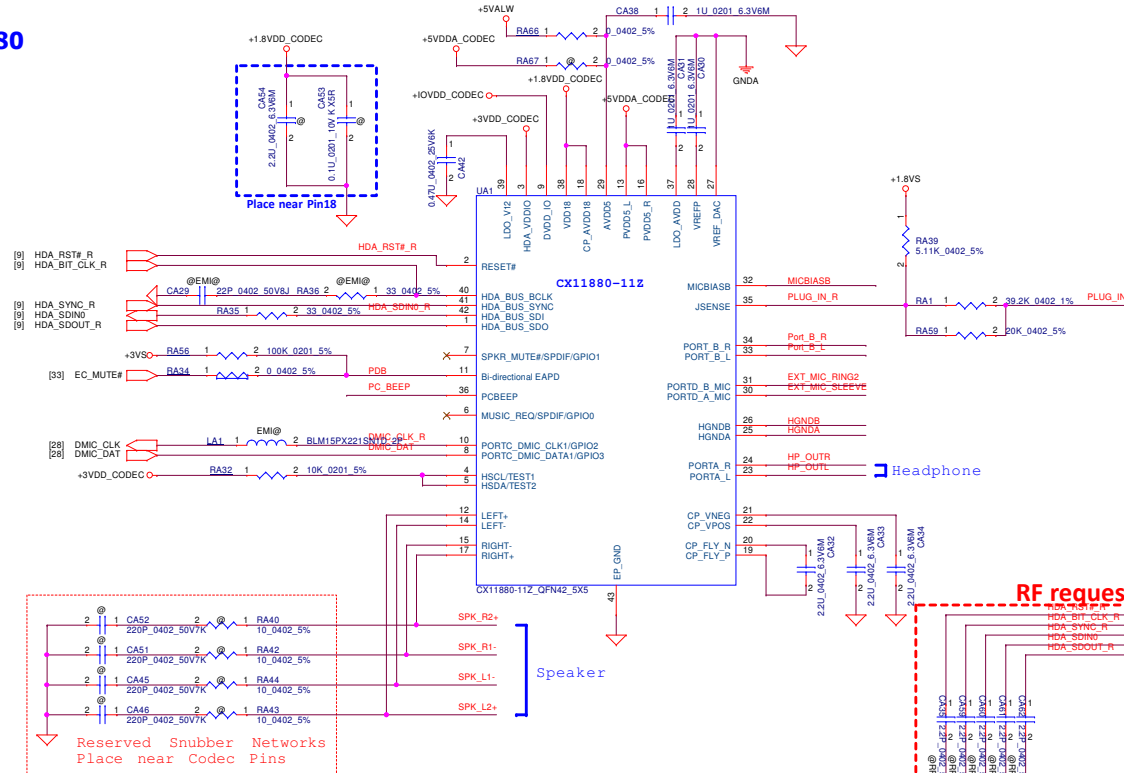
NGFF_SSD_PEDET#
H : PCIE Interface
L : SATA Interface
Fellow 543016_SKL_U_Y_PDG_0_9

SSD(TYPE M)

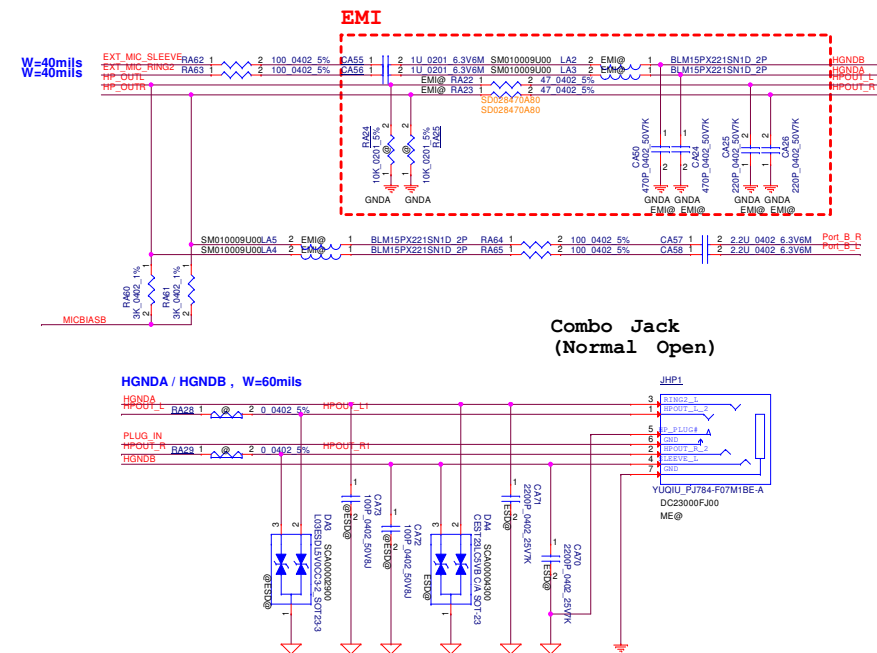
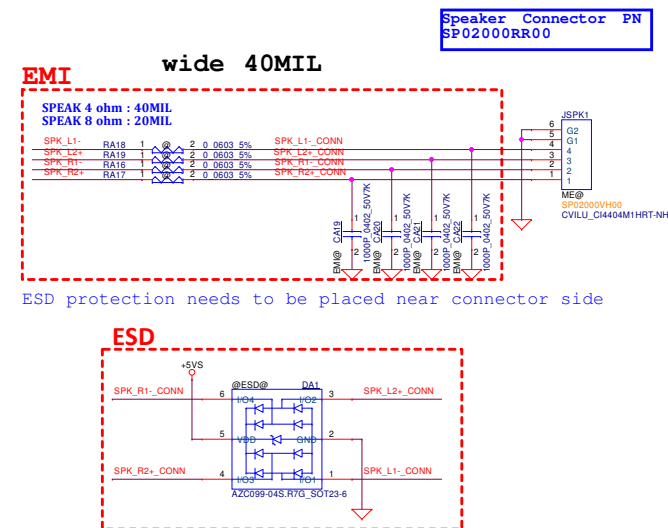


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Size	Document Number	LA-H081P		Rev
C				0.2
Date: Monday, October 22, 2018		Sheet	31	of 53

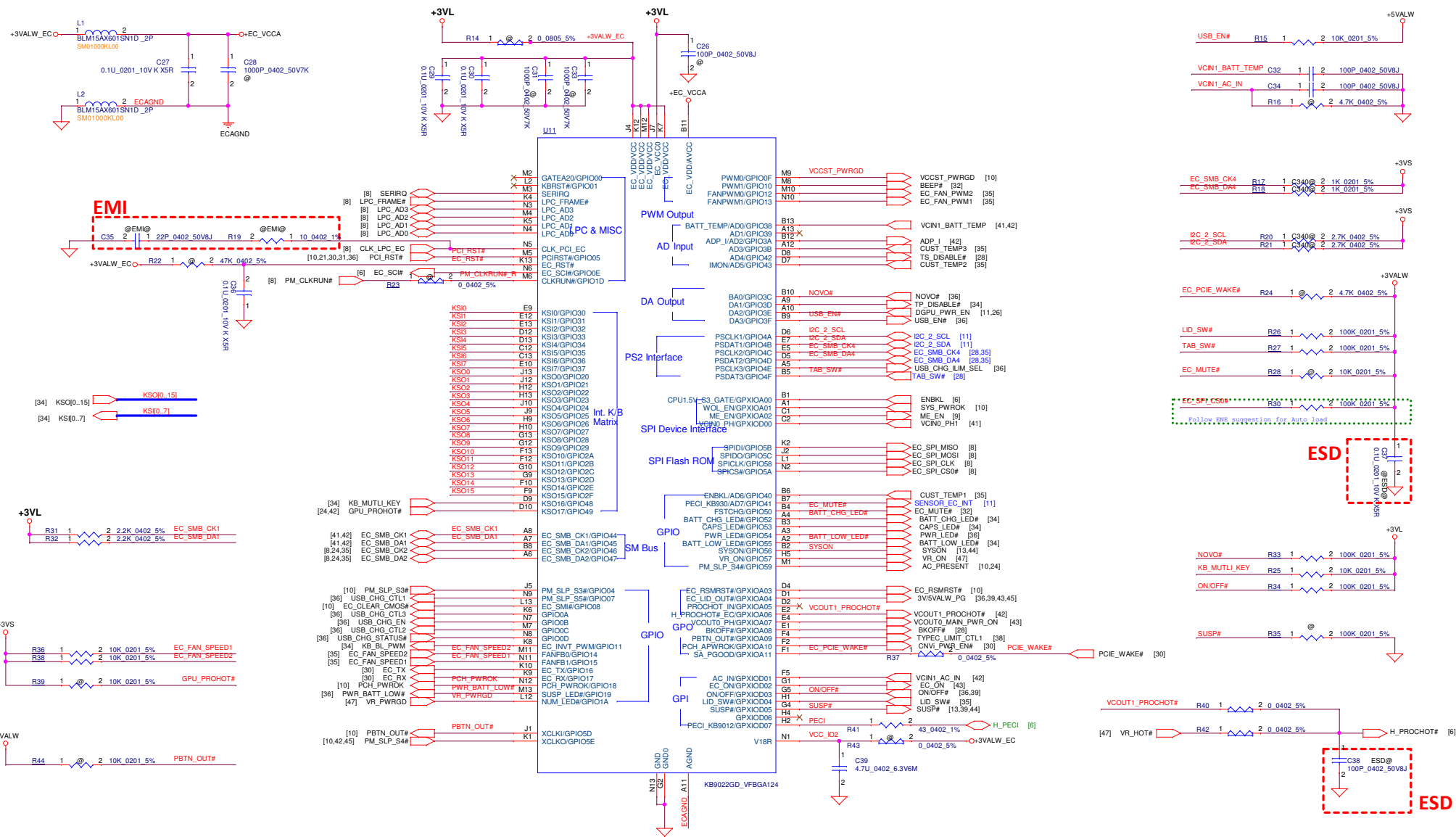
CX11880



Speaker



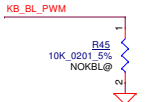
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/05/04	Deciphered Date	2019/04/09	Title	HD Audio Codec_CX11880
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				Document Number	0.2
				Custian	LA-H081P
Date:	Tuesday, October 23, 2018	Sheet	32	of	53



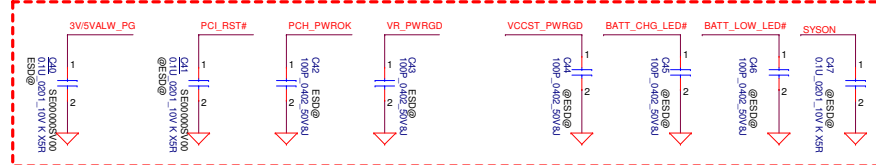
Keyboard BackLight_SELECT

Function	KBL_ID
KBL	1
NO KBL	0

PH on KB side

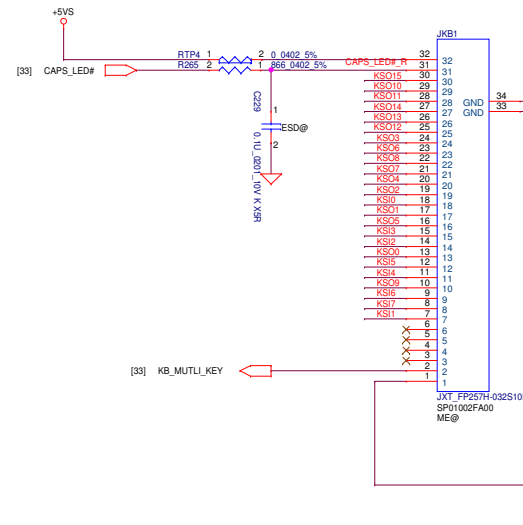
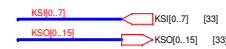
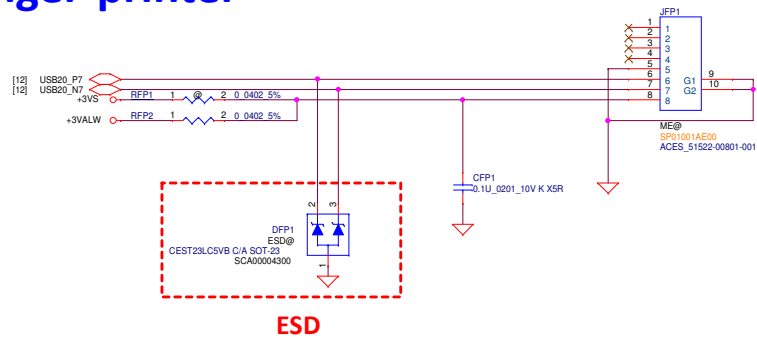


ESD

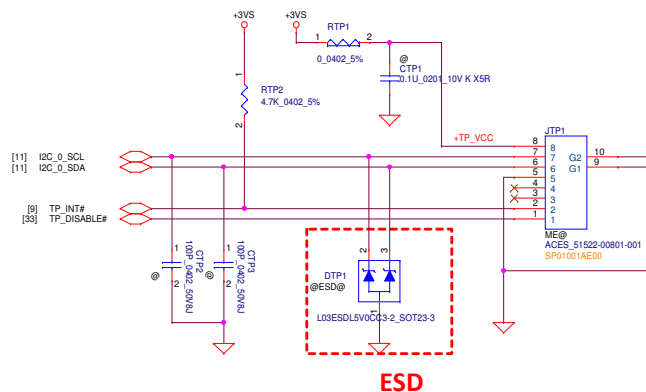


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				Custom: LA-H081P	
				Date: Monday, October 22, 2018	Sheet 33 of 53

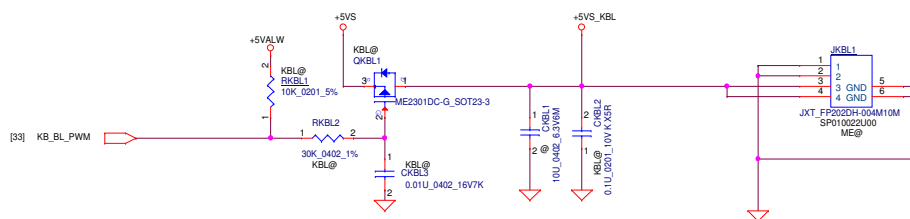
Keyboard



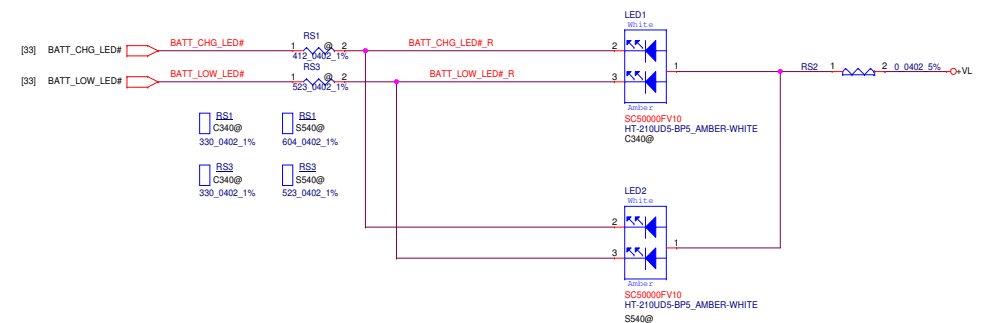
Touch Pad



Keyboard Backlight

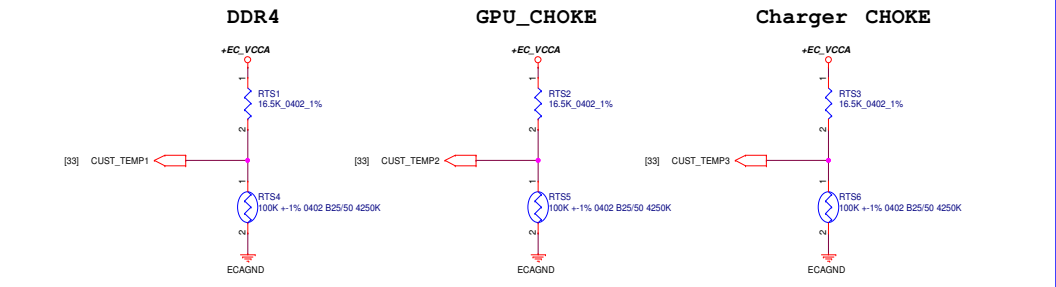
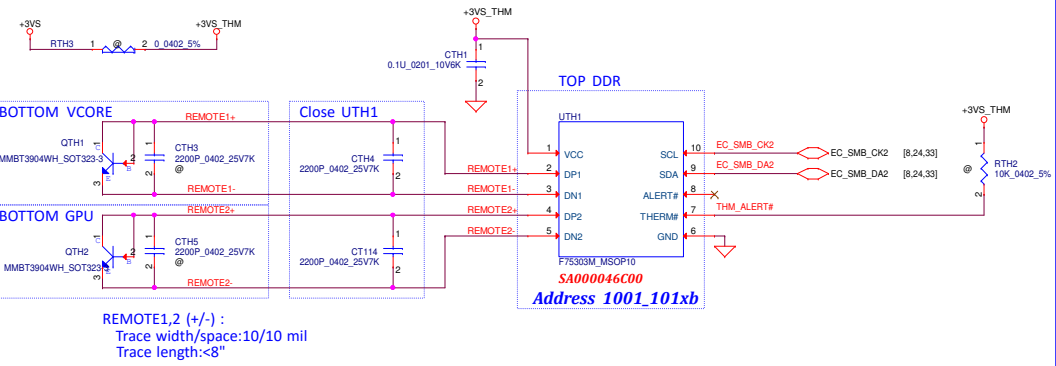


BATT LED

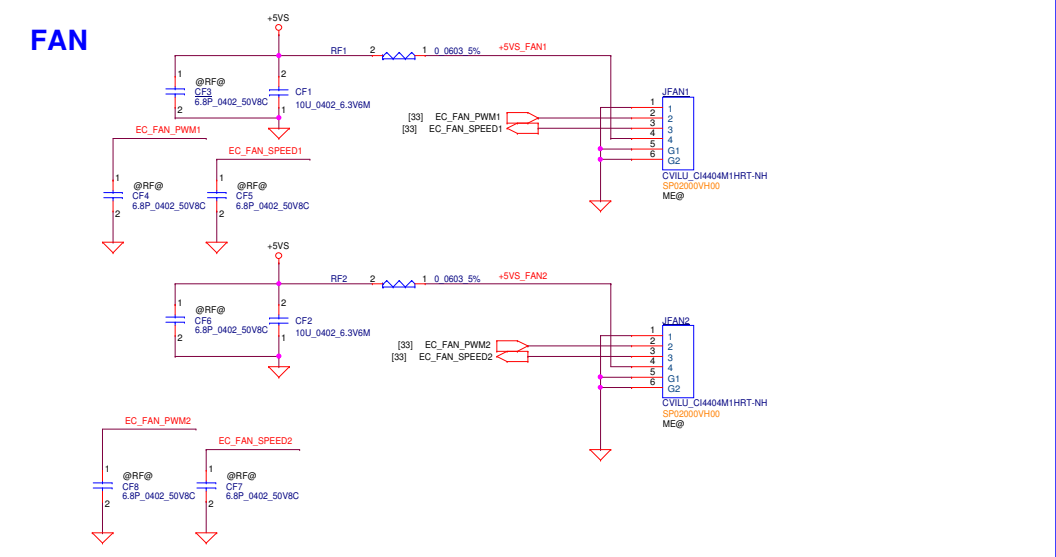


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Issued Date	2017/5/3	Deciphered Date	2019/04/09	Title		
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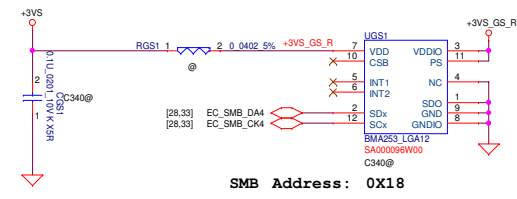
THERMISTOR



FAN

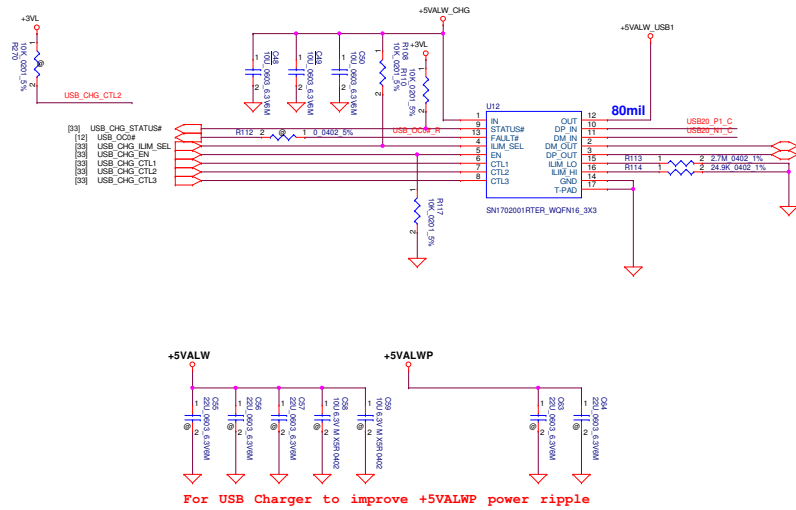


G-Sensor

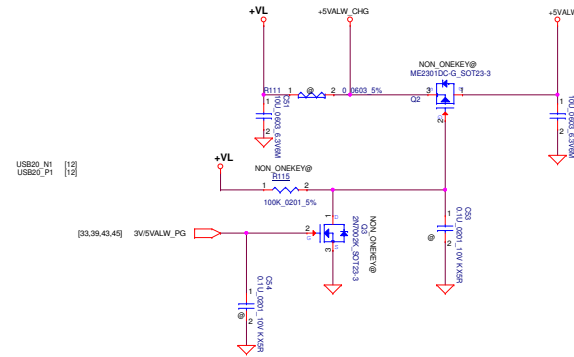


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Issued Date	2017/5/3	Deciphered Date	2019/04/09	Title
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Size	Document Number	LA-H081P		Rev 0.2
Date: Monday, October 22, 2018	Sheet	35	of	53

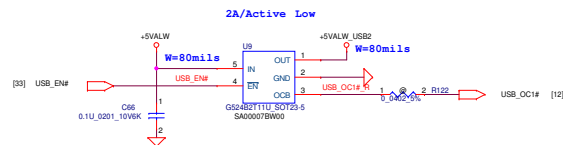
USB3.0_Port (AOU_Port)



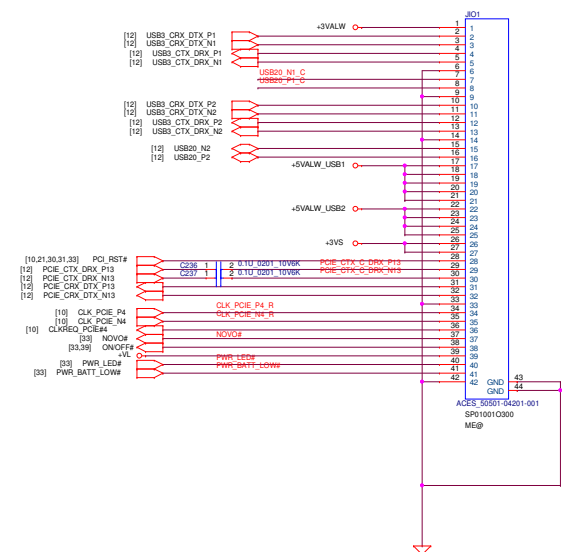
USB Charge switch



USB3.0_Port















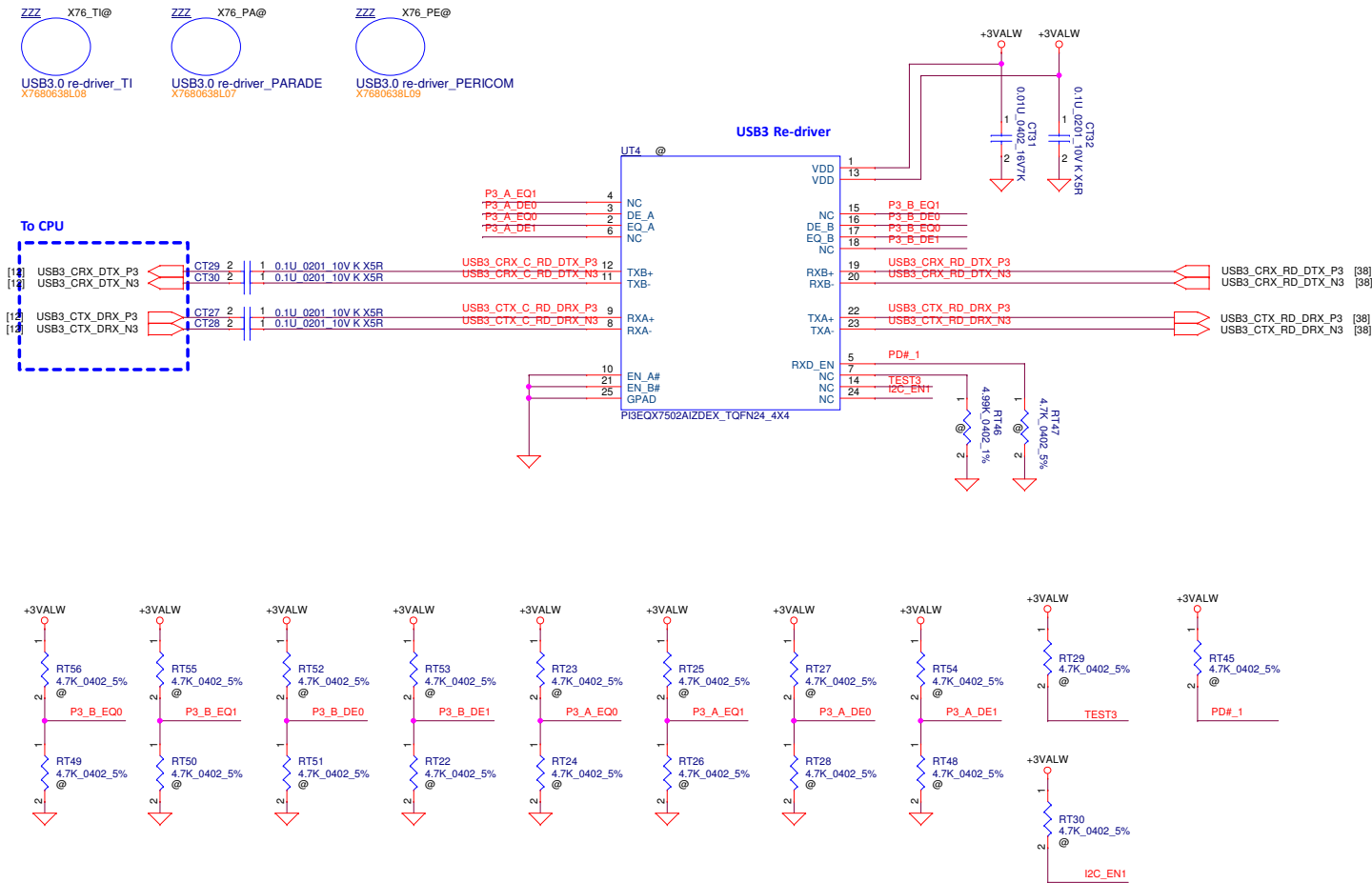
I/O CONN



Security Classification	Compul Secret Data		Title	
Issued Date	2018/04/06	Deciphered Date	2018/04/09	Compul Electronics, Inc. IO board
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			Customer	LA-H081P
Date:	Monday, October 29, 2018	Sheet	36	of 53

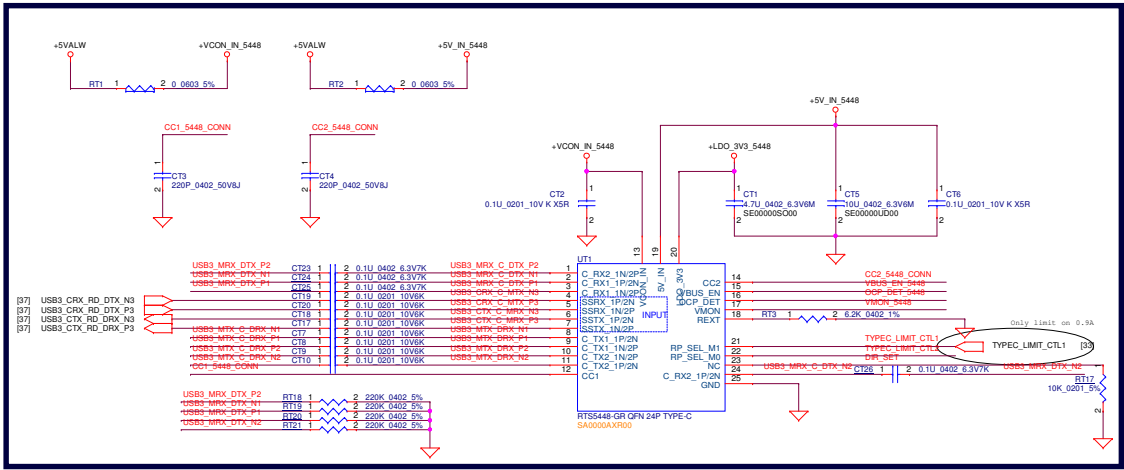
USB3.0_Port

TI @	 UT4 TI@ SN63LPVES02ARGER	 RT48 TI@ 0.0402_5%	 RT22 TI@ 0.0402_5%	 RT49 TI@ 4.7K_0402_5%	 RT50 TI@ 4.7K_0402_5%	 RT51 TI@ 4.7K_0402_5%
PA@	 UT4 PA@ PSB713BTQFN24GTR2-A2	 RT25 PA@ 4.7K_0402_5%				
PE@	 UT4 PE@ PI9EX7550AIZDEX TQFN24	 RT49 PE@ 4.7K_0402_5%	 RT24 PE@ 4.7K_0402_5%	 RT28 PE@ 4.7K_0402_5%		

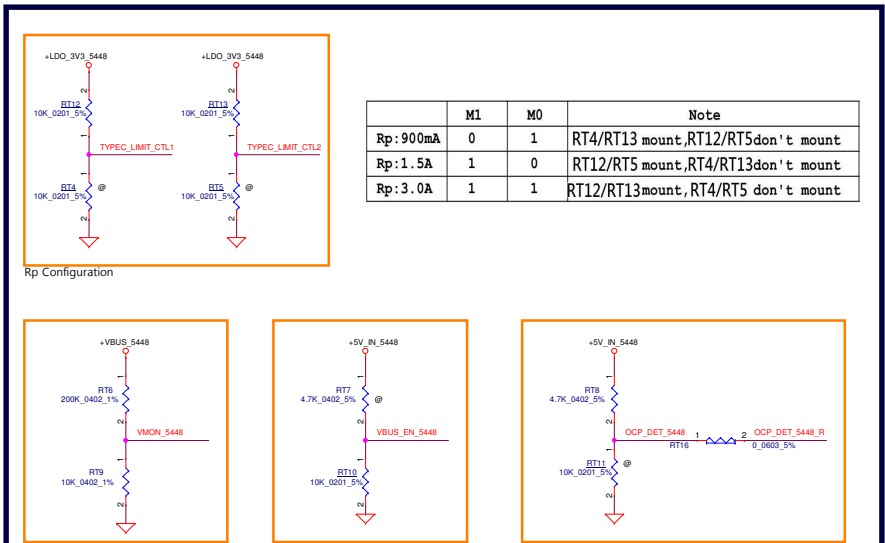


Security Classification	Compal Secret Data					
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	Type-C USB redriver	
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					LA-H081P	0.2
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TYPE-C - CC+MUX (RTS5448-GR)



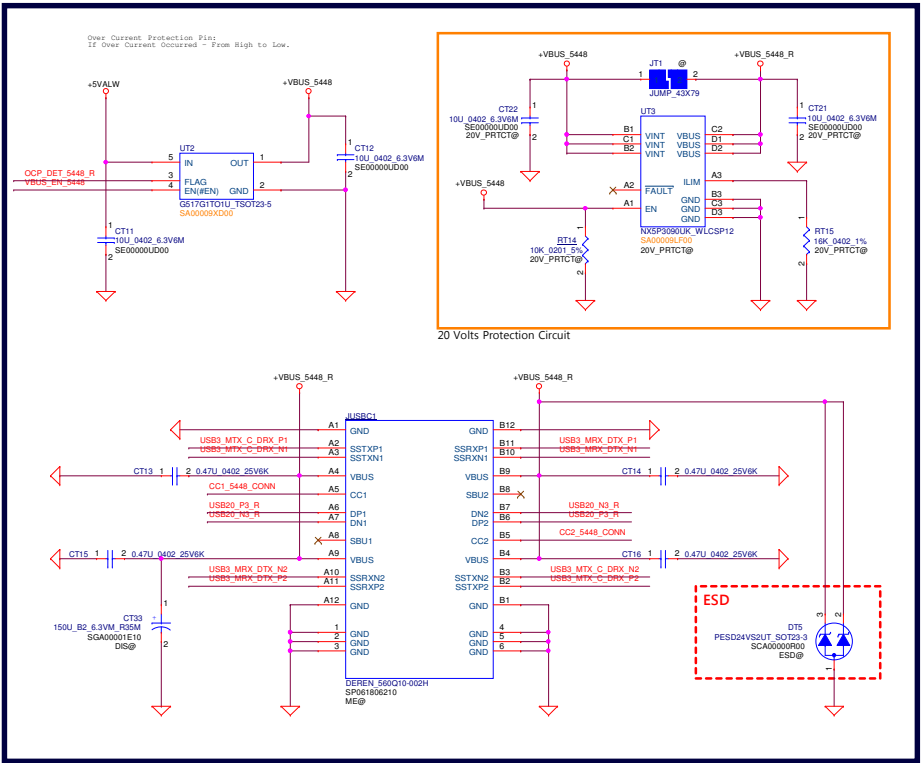
MUX MISC.



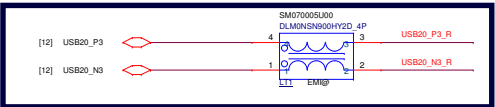
Power switch enable pin	Note
Low Active	RT7/RT10 mount
High Active	RT10 mount, RT7 don't mount

Power switch OCP pin	Note
Low Active	RT8/RT11 mount
High Active	RT11 mount, RT8 don't mount

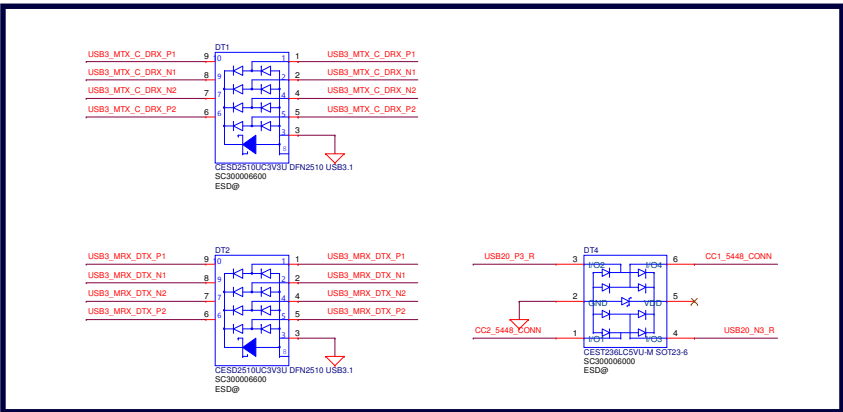
TYPE-C CONNECTOR



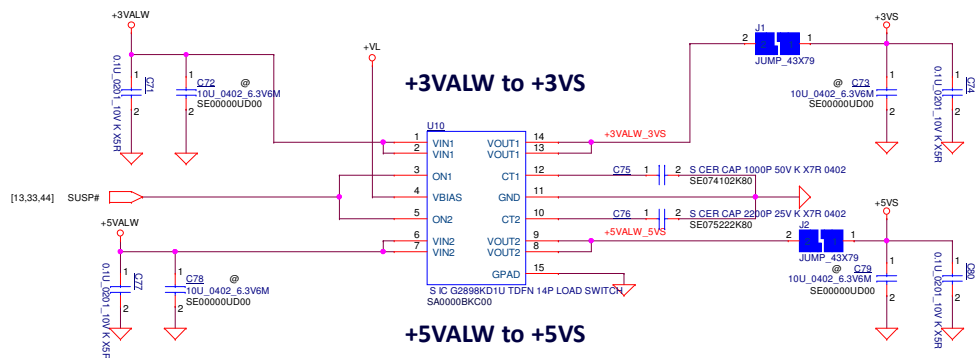
USB2.0



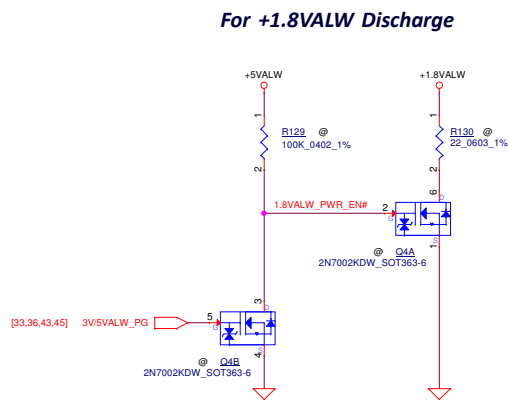
ESD COMPONENTS



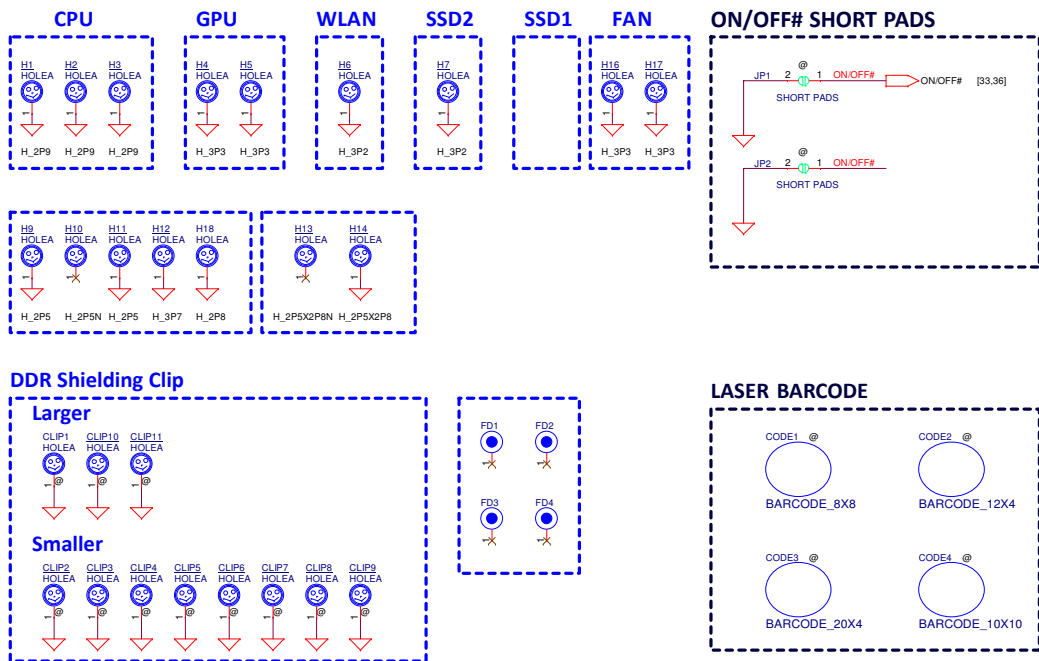
DC to DC



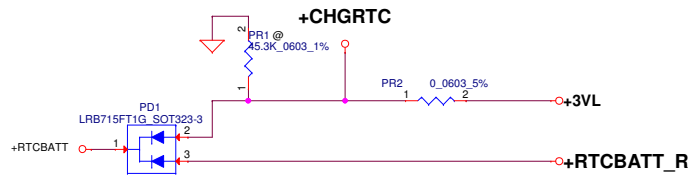
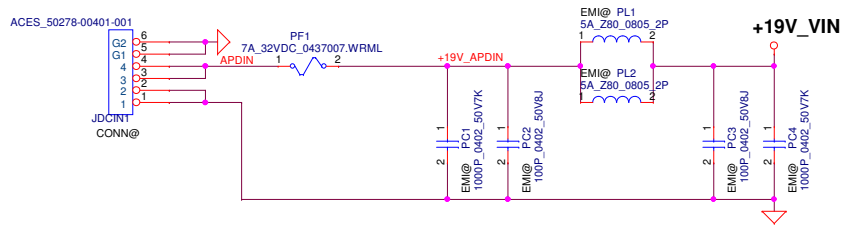
DISCHARGE CIRCUIT



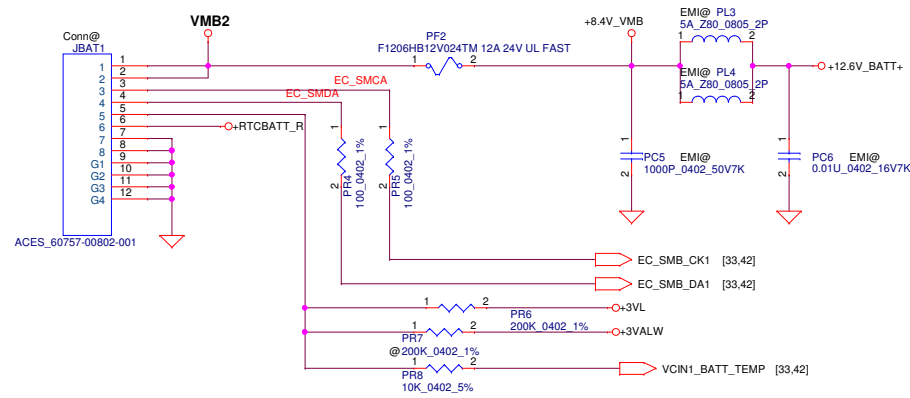
MISC.



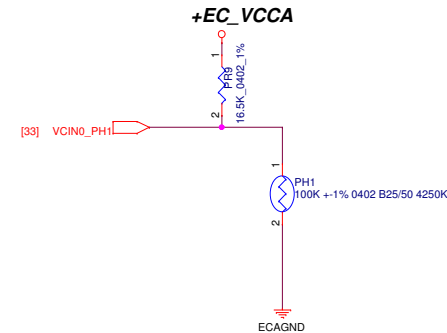
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Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	DC to DC / Discharge / MISC
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				Date:	Monday, October 22, 2018
				Sheet	39 of 53



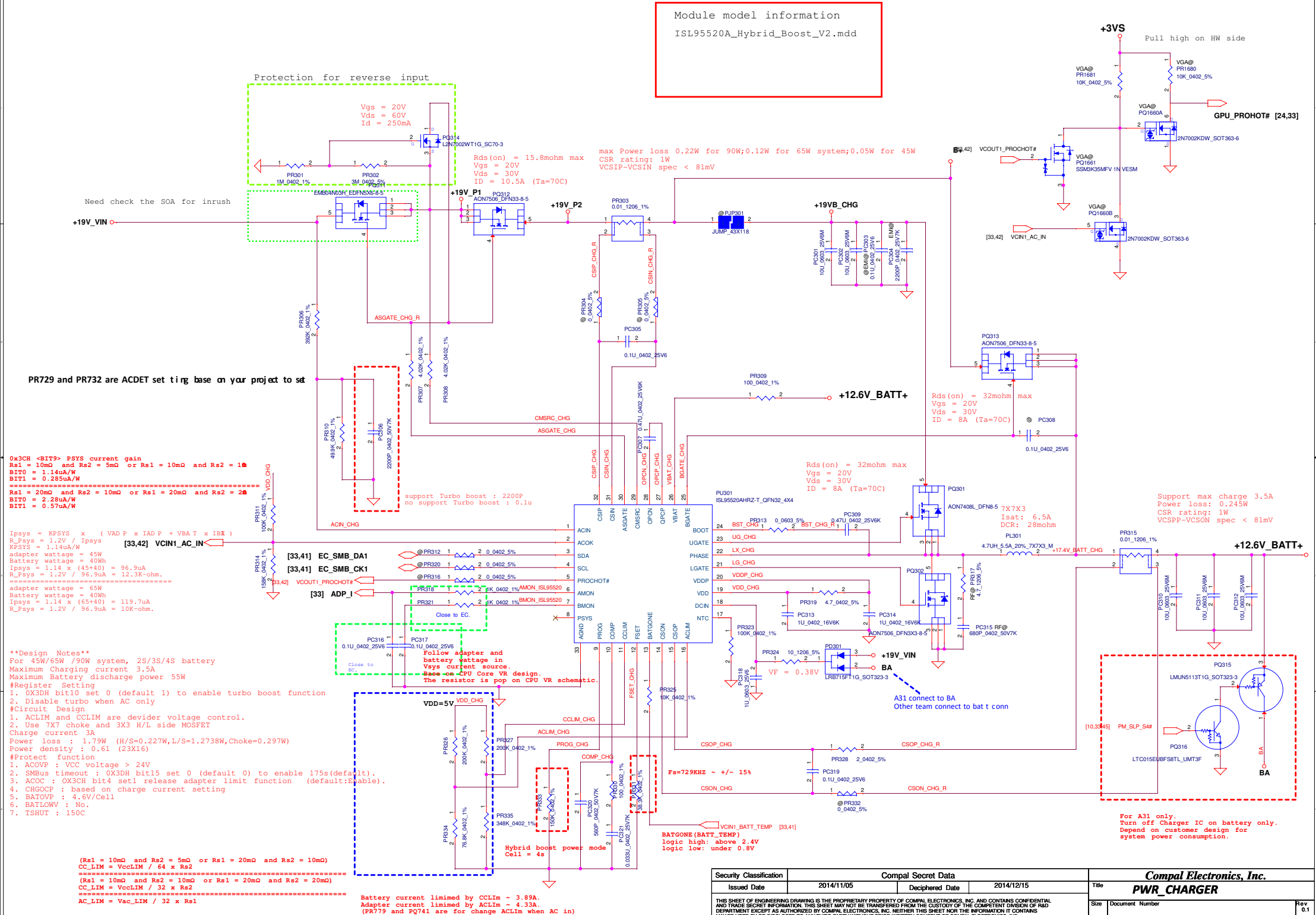
Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2018/04/09		Deciphered Date		2019/04/09		Title		
								PWR- DCIN / Vin Detector		
								Size		Rev
								Document Number		0.1
								KBL		
								Date: Monday, October 22, 2018		
								Sheet 40 of 53		



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



```
Module model information
ISL95520A_Hybrid_Boost_V2.mdd
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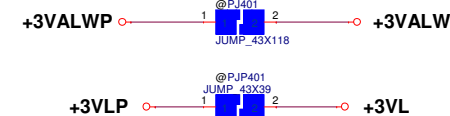
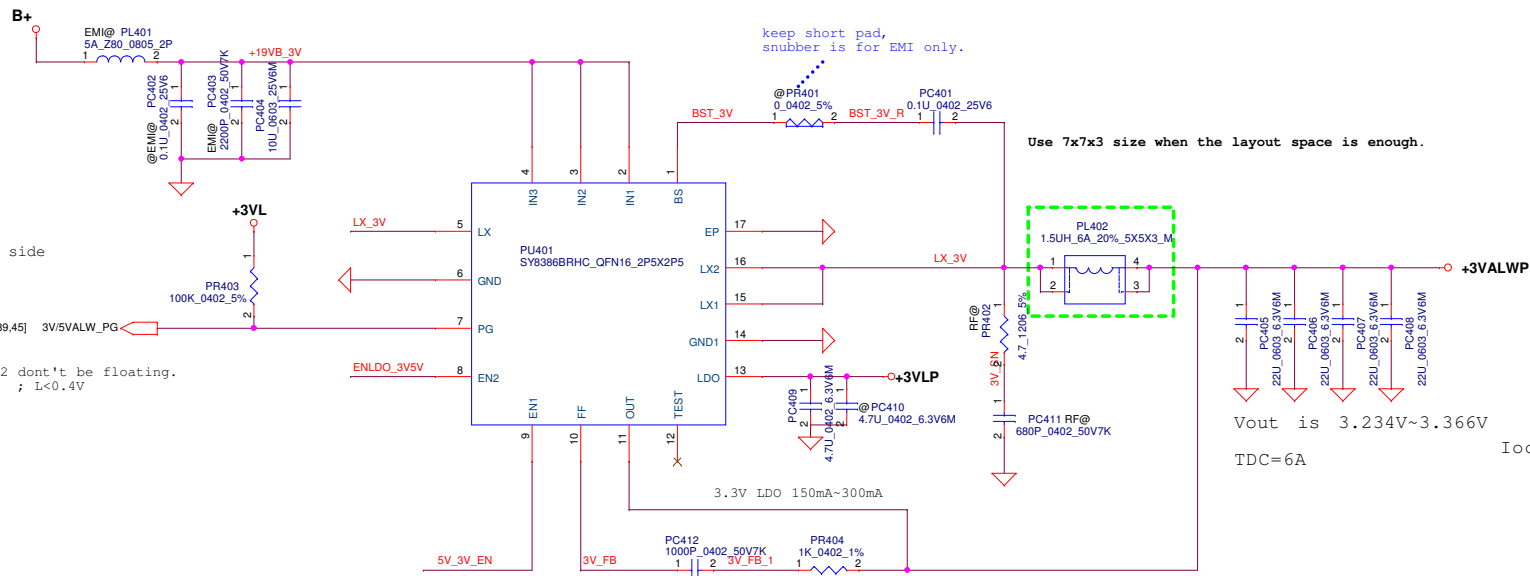


Module model information

SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd

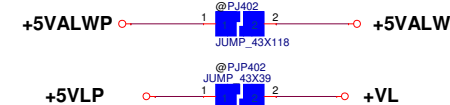
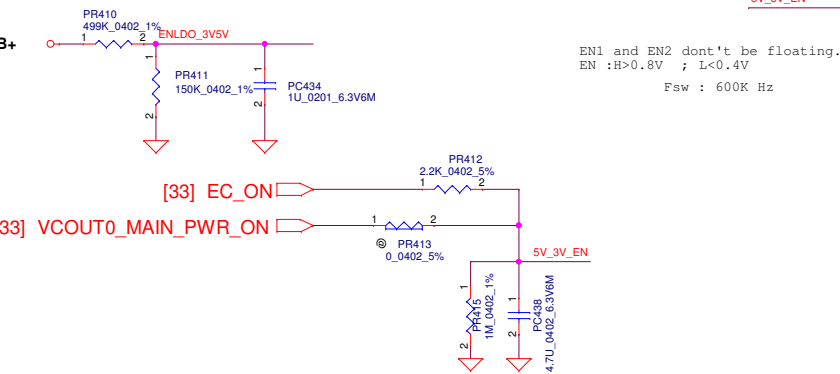
Check pull up resistor of SPOK at HW side

Fsw : 600K Hz EN1 and EN2 don't be floating.
EN :H>0.8V ; L<0.4V



Module model information

SY8286C_V3_single.mdd
SY8286C_V3_dual.mdd



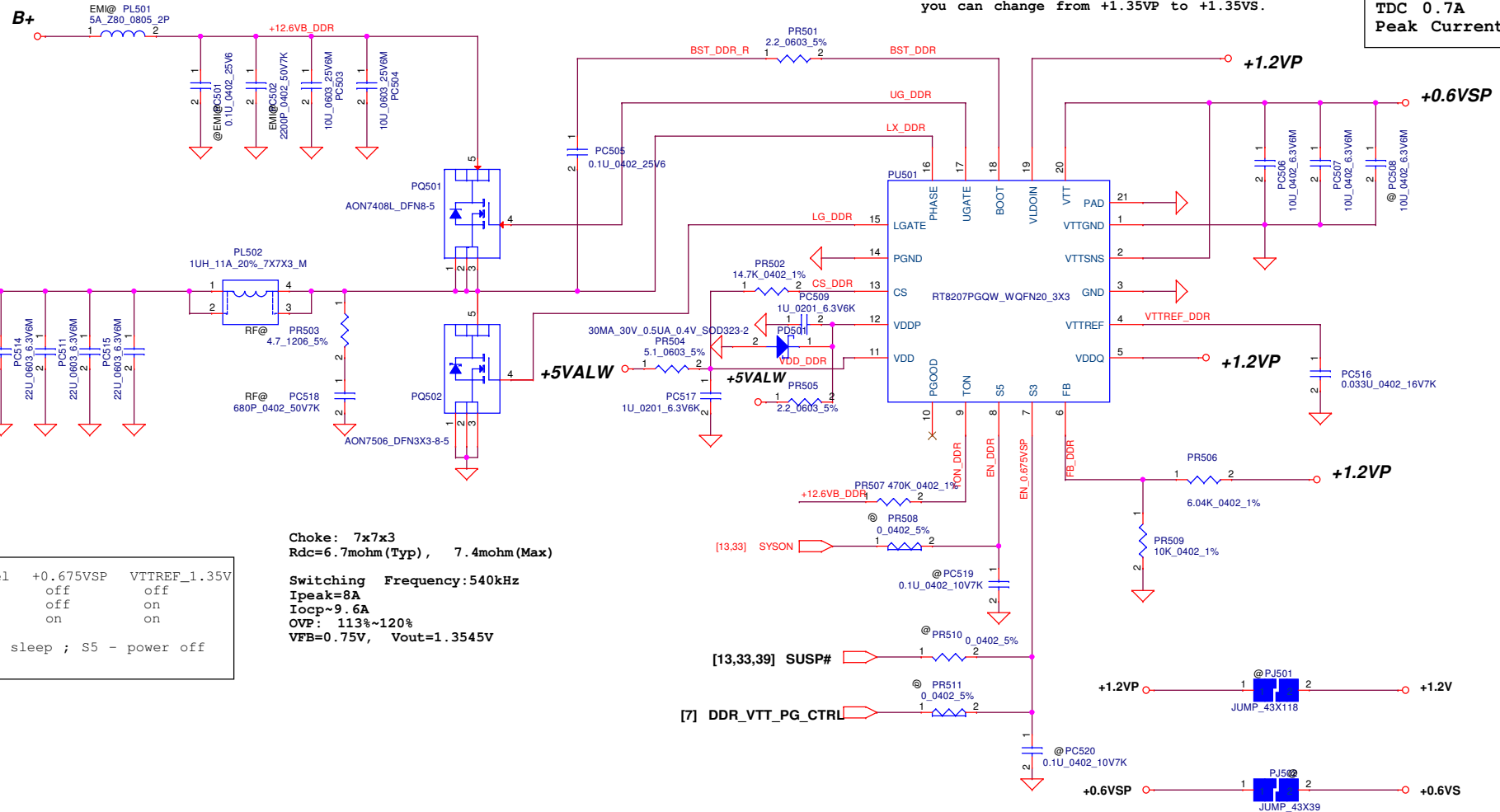
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Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

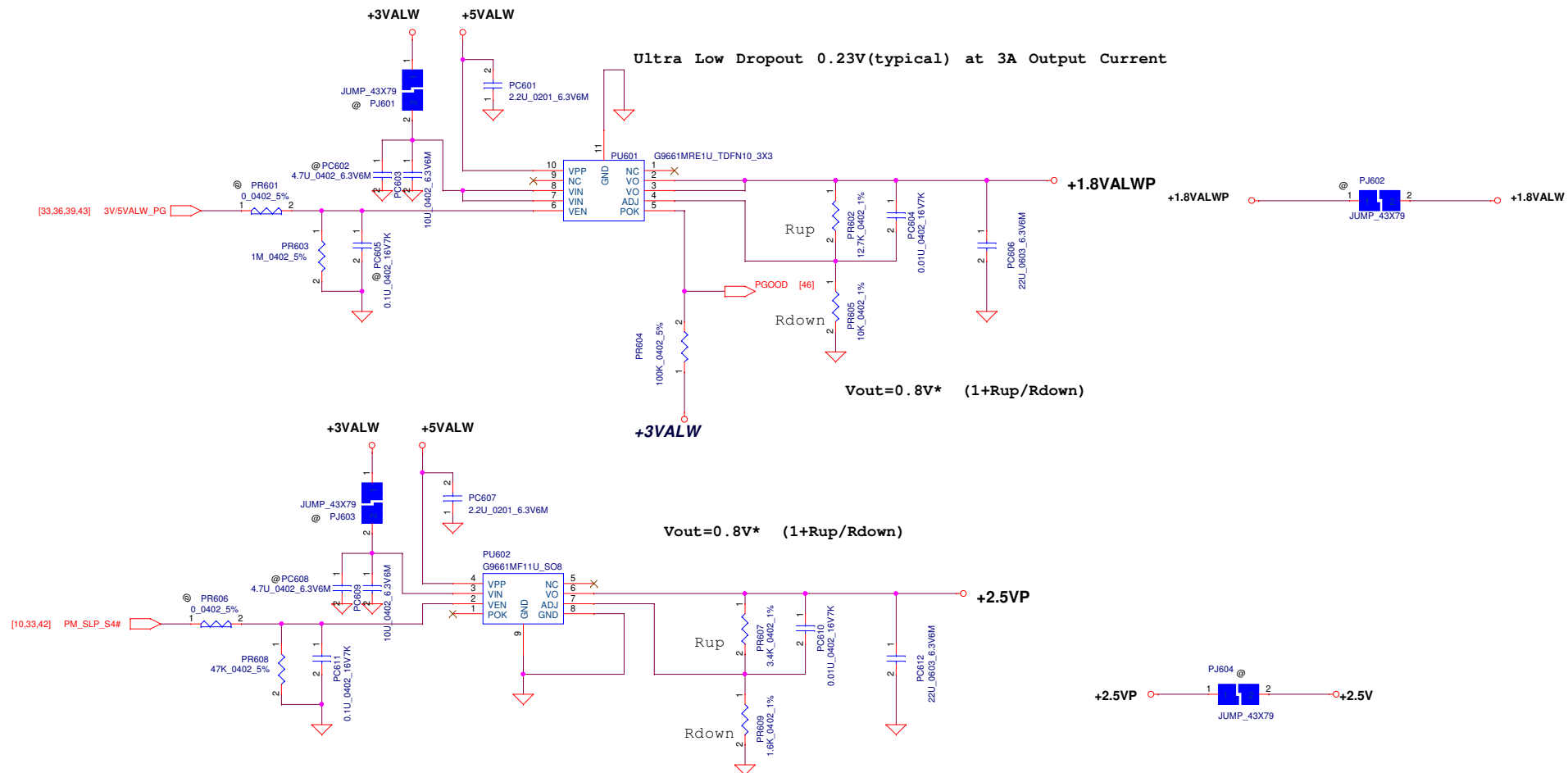
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



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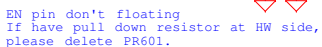
Module model information

APL5930_V2.mdd

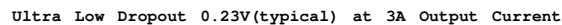


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SY8286_V2_single.mdd
SY8286_V2_dual.mdd

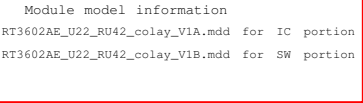


The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

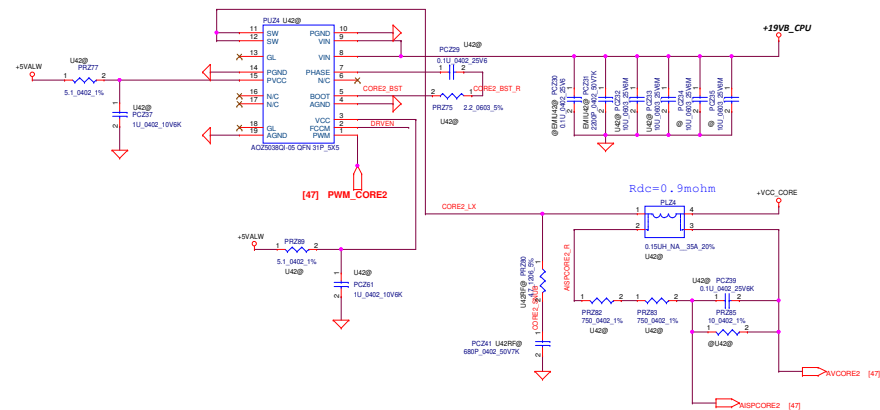


$$\begin{aligned} V_{out} &= 0.8V * (1 + R_{up}/R_{down}) \\ &= 0.8 * (1 + (10/38.3)) \\ V_{out} &= 1.008V \end{aligned}$$

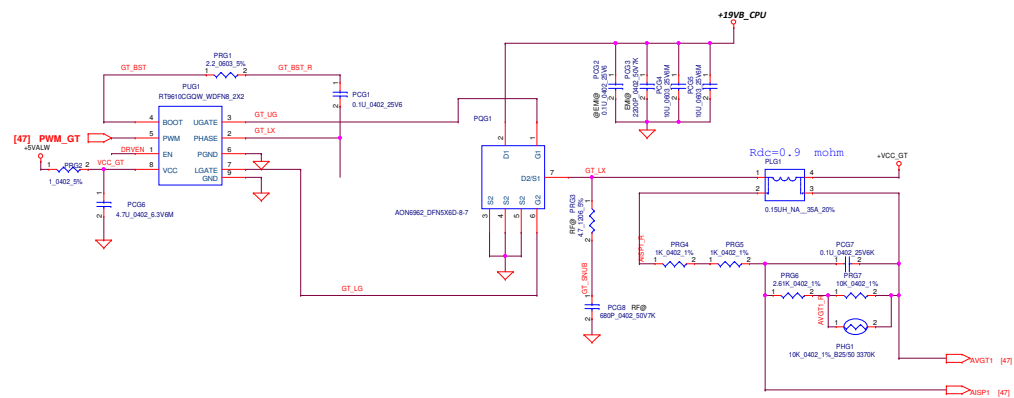
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	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A



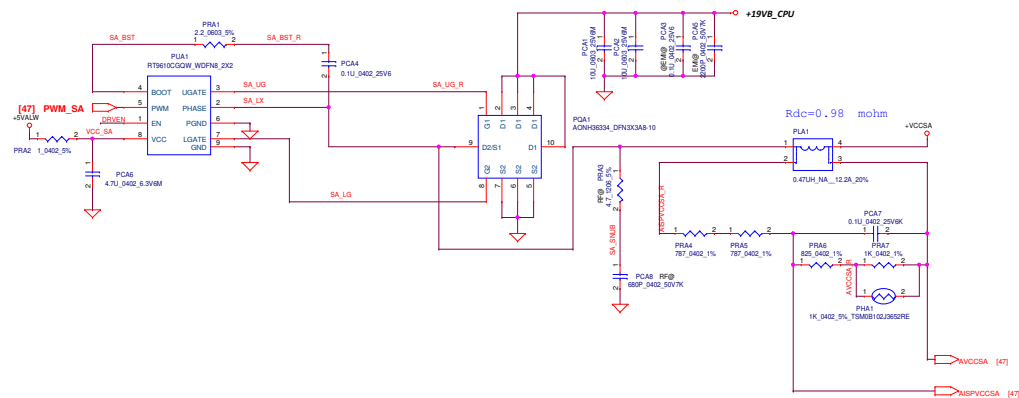
```
L/S AON6214:
R DS(ON)    (at V GS =10V) < 2.8m?
R DS(ON)    (at V GS =4.5V) < 3.5m?
```



VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

```
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A
```

```
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A
```

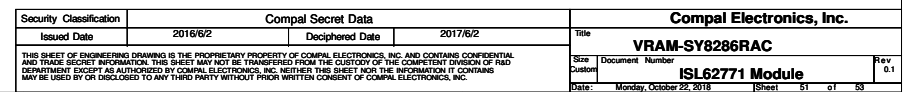


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2017/06/06
VCORE Output Capacitor:
U42
22uF_0603*41
1uF_0201*35
330uF *2
UNPOP
22_0603*1

SY8286_V1_single.mdd
SY8286_V1_dual.mdd



Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	To avoid shortage issue and fix BOM error		Add PR407(SD028000080,S RES 1/16W 0 +-5% 0402) Change PQ1661 PN from SB000012900 to SB000011Z00	2018/07/31	EVT
2	Modify BOM for X1 code		Change PQ314 from SB00000ST00 to SB000009Q80	2018/08/10	DVT
3	Modify BOM for X1 code		Change PC315,PC411,PC702,PC1202 from 680P_0603_50V7K to 680P_0402_50V7K	2018/08/10	DVT
4	Modify Vin detector setting for 4 cell battery		Change PR306 from 287K_0402_1% to 392K_0402_1%	2018/08/16	DVT
5	Change Battery connector P/N		Change JBATT1 to ACES 60757-00802-001	2018/08/16	DVT
6	Change +3VALWP IC solution		Change PU401 from SY8286BRAC to SY8386BRHC	2018/08/16	DVT
7	Change +1.05VALWP & +1.35VGSP IC solution		Add PR1209(SD034100180,S RES 1/16W 1K +-1% 0402) Change PU701 & PU1201 from SY8286RAC to SY8386RHC	2018/08/16	DVT
8	Charger IC Vendor suggestion		Change PR330 from 349_0402_1% to 100_0402_1% Change PC321 from 0.015U_0402_25V7K to 0.033U_0402_25V7K Change PR333 from 182K_0402_1% to 150K_0402_1%	2018/08/27	DVT
9	Follow cost down action		Change PC9120,PC9126,PC9127,PC9129 from 0.47U_0201_4V6M to 0.47U_0201_6.3V6K	2018/08/27	DVT
10	Change PQ311 P/N		Change PQ311 P/N from SB00001IL00 to SB00001C500	2018/08/27	DVT
11	Charger IC Vendor suggestion		PC307 & PC309 change from SE000005Z80(S CER CAP 0.22U 25V K X7R 0603) to SE00000WA00(S CER CAP 0.47U 25V K X5R 0402)	2018/08/27	DVT
12	Follow cost down action		PCZ19 change from SE000013J00(S CER CAP 0.22U 25V K X6S 0402) to SE000015W00(S CER CAP 0.22U 25V K X5R 0402)	2018/08/27	DVT
13	Follow cost down action		PCZ3,PCZ13,PCZ16 change from SE074104K80(S CER CAP 0.1U 50V K X7R 0402) to SE00000G880(S CER CAP 0.1U 25V K X5R 0402)	2018/08/27	DVT
14	Follow cost down action		PC505 , PC1204 change from SE00000W210(S CER CAP 0.1U 25V K X7R 0402) to SE00000G880(S CER CAP 0.1U 25V K X5R 0402)	2018/08/27	DVT
15	Fine tune for U42 CPU transient test result		Add PC9103, PC9187 ,PC9188 ,PC9189(22U_0603_6.3V6M)	2018/08/29	DVT
16	Follow HW request		Change PR826 from 100K to 10K	2018/08/29	DVT
17	Fine tune for U42 CPU transient test result		Change PRZ35 from 4.22K to 2.8K Change PRZ71 from 182K to 19.1K Change PCZ11 from 150p to 330p Change PRZ48 from 30K to 28K Change PRZ67 from 115 to 7.68K Change PRZ54 from 22.1K to 24.3K Change PRZ70 from 549K to 5.62K Change PRZ68 from 374 to 4.64K	2018/08/30	DVT
18	Fine tune for U22 CPU transient test result		Delete PC9101,PC9166,PC9167,PC9168,PC9169,PC9170,PC9171,PC9068,PC9080,PC9002,PC9003,PC9027,PC9034 for U22 CPU SKU	2018/09/05	DVT
19	To avoid RTC loos issue		Delete PR1(45.3K_0603_1%) Change PR2 from 1.5K_0603_1% to 0_0603_5%	2018/09/06	DVT
20	0 ohm change to short pad		Change PR304,PR305,PR332,PR407,PR413,PR508,PR511,PR709, PR601, PR606,PR705, PR711,PR803 to short pad	2018/10/11	PVT

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